BOOTLOADER MANUAL

PEC Series

AC-DC & DC-DC
CRPS Front End Power Supplies

belfuse.com/power-solutions

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1. BOOTLOADER FUNCTION DESCRIPTION

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). It is desired that any other microcontroller in the power supply also be able to be updated with this same process (example: primary side microcontroller); however, this is not a requirement at this time.

2. FW IMAGE MAPPING

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1) Boot Loader:
This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).

2) Main Program:
This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

3. POWER SUPPLY OPERATING MODE DURING AND AFTER FIRMWARE UPDATE

1) Firmware update mode in ON state with no power cycle needed:
Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

2）Bad image after firmware update:
The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

4. FIRMWARE IMAGE HEADER

4.1 PEC550 SERIES

4.1.1 PEC550-12-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	5	
Byte 15	5	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	N	
Byte 21	A	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.1.2 PEC550-12-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	5	
Byte 15	5	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	R	
Byte 21	A	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.1.3 PEC550-12-074ND FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	5	
Byte 15	5	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	N	
Byte 21	D	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.1.5 PEC550-12-074RD FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	5	
Byte 15	5	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	R	
Byte 21	D	
Byte 22		
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Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.2 PEC800 SERIES

4.2.1 PEC800-12-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	8	
Byte 15	0	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	N	
Byte 21	A	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.2.2 PEC800-12-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	8	
Byte 15	0	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	R	
Byte 21	A	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
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Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.2.3 PEC800-12-074ND FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	8	
Byte 15	0	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	N	
Byte 21	D	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
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Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.2.4 PEC800-12-074RD FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	8	
Byte 15	0	
Byte 16	0	
Byte 17	-	
Byte 18	1	
Byte 19	2	
Byte 20	R	
Byte 21	D	
Byte 22		
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.3 PEC1300 SERIES

4.3.1 PEC1300-12-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	3	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	N	
Byte 22	A	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.3.2 PEC1300-12-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	3	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	R	
Byte 22	A	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.3.3 PEC1300-12-074ND FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	3	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	N	
Byte 22	D	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.3.4 PEC1300-12-074RD FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	3	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	R	
Byte 22	D	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.4 PEC1600 SERIES

4.4.1 PEC1600-12-074NA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	6	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	N	
Byte 22	A	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.4.2 PEC1600-12-074RA FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	6	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	R	
Byte 22	A	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.4.3 PEC1600-12-074ND FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	6	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	N	
Byte 22	D	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

4.4.4 PEC1600-12-074RD FIRMWARE IMAGE HEADER

Byte 1	CRC Low Byte	Supplier internal use area 10 bytes
Byte 2	CRC High Byte	
Byte 3	Image Offset Low Byte	
Byte 4	Image Offset High Byte	
Byte 5	Image Size Low Byte	
Byte 6	Image Size High Byte	
Byte 7	Image Sector ID Low Byte	
Byte 8	Image Sector ID High Byte	
Byte 9	Image Update Key Low Byte	
Byte 10	Image Update Key High Byte	
Byte 11	P	Model Name 12 bytes
Byte 12	E	
Byte 13	C	
Byte 14	1	
Byte 15	6	
Byte 16	0	
Byte 17	0	
Byte 18	-	
Byte 19	1	
Byte 20	2	
Byte 21	R	
Byte 22	D	
Byte 23	Not used, for future use	Not used, for future use
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).	Firmware Revision 3 bytes; in binary format
Byte 25	FW_MINOR_PRIMARY (not used by system)	
Byte 26	FW_MINOR_SECONDARY	
Byte 27	HW_REVISION_FIRST	Hardware Compatible Revision 2 bytes
Byte 28	HW_REVISION_SECOND	
Byte 29	BLOCK SIZE Low Byte	
Byte 30	BLOCK SIZE High Byte	
Byte 31	Write Time Low Byte	
Byte 32	Write Time High Byte	

5. FIRMWARE UPDATE PROCESS

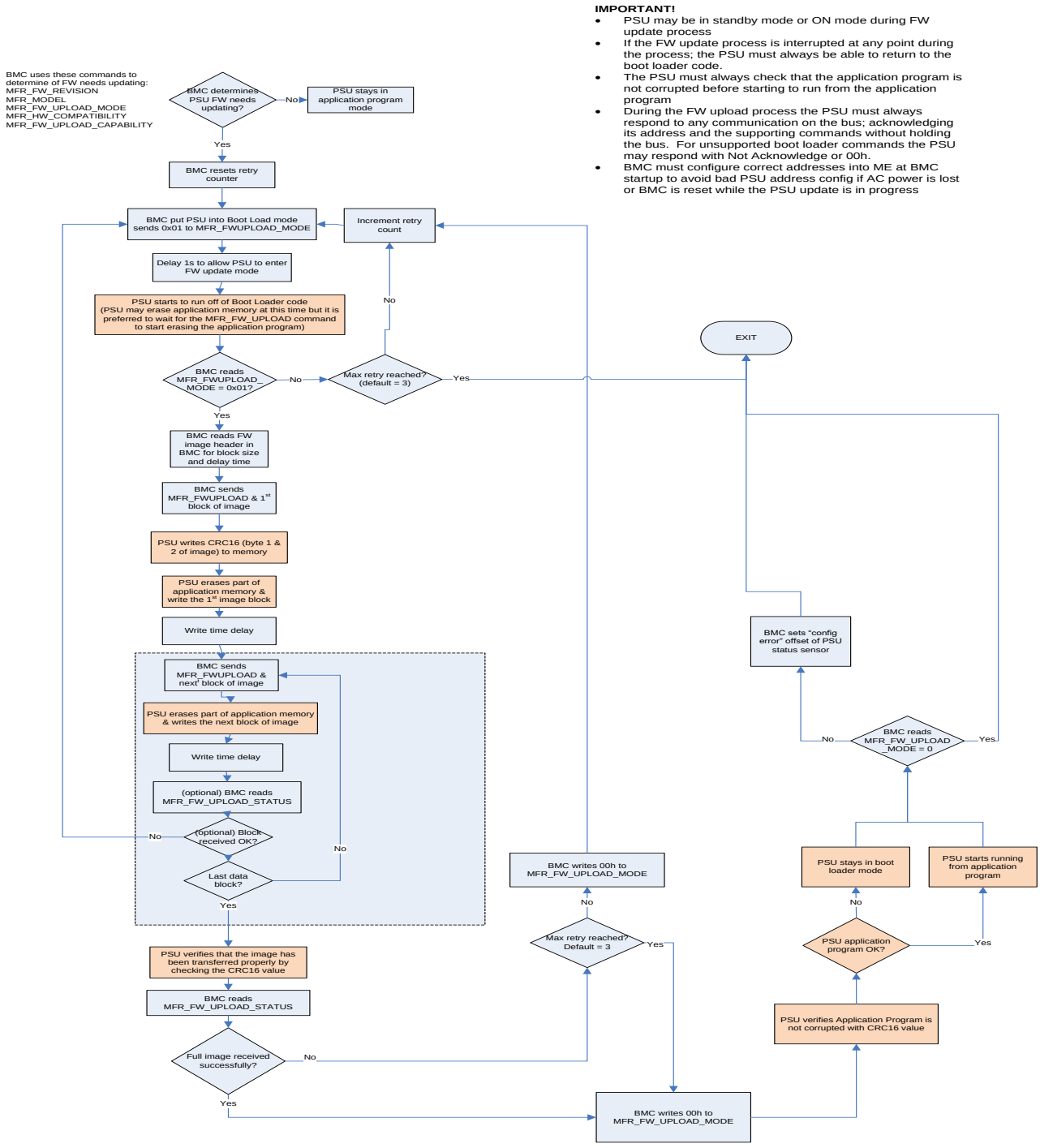

Figure 1. PSU Upload Process

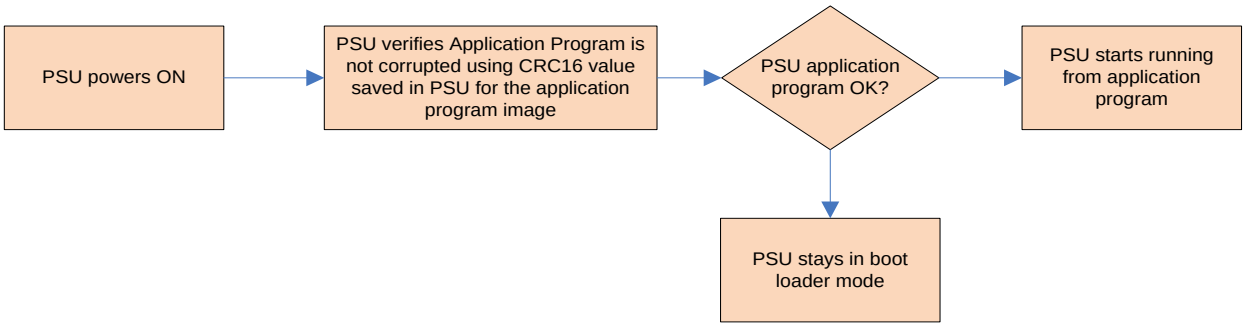

Figure 2. PSU flow during powering ON

6. RELATED COMMAND OF BOOTLOADER

6.1 Name: MFR_HW_COMPATIBILITY

Format: Read Word

Code: D4h

BYTES	VALUE	DESCRIPTION
low	ASCI code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

6.2 Name: MFR_FWUPLOAD_CAPABILITY

Format: Read Byte

Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

BIT	VALUE	DESCRIPTION
0 (for future use)	1 = PSU support FW uploading in standby mode only	For future use
1(for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

6.3 Name: MFR_FWUPLOAD_MODE

Format: Read/Write Byte

Code: D6h

BIT	VALUE	DESCRIPTION
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

6.4 Name: MFR_FWUPLOAD

Format: Block Write (block = size as defined by the image header)

Code: D7h

BYTES	VALUE	DESCRIPTION
Block size defined in header	Image header & image data	Command used to send each block of the FW image. Header should follow the format described in section 13.4. The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

6.5 Name: MFR_FWUPLOAD_STATUS

Format: Read Word

Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to '0' when the power supply enters FW upload mode.

BIT	DESCRIPTION
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

6.6 Name: MFR_FW_REVISION

Format: Block Read, 3 bytes

Code: D9h

BYTE	VALUE	DESCRIPTION
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW has to be avoided. System BMC can elect to ignore this bit if needed, but recommended to follow. 0→ No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version. Bit 0-6: Major revision

6.7 MFR_MODEL (existing Power Management Bus command)

Code: 9Ah

Maximum of 12 byte value; ending in terminator character.

6.8 MFR_REVISION (existing Power Management Bus command)

Code: 9Bh

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
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