ELECTRICAL SPECIFICATIONS:

1.0 TURNS RATIO: (P6–P5–P4) : (J6–J3)  
   (P3–P2–P1) : (J2–J1)  
   : 1CT : 1CT ± 3%
   : 1CT : 1CT ± 3%

2.0 INDUCTANCE: (P6–P4)  
   (P3–P1)  
   : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
   : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias

3.0 LEAKAGE INDUCTANCE: P6–P4 (WITH J6 AND J3 SHORT)  
   P3–P1 (WITH J2 AND J1 SHORT)  
   : 0.3 MAX. @ 1MHz

4.0 INTERWINDING CAPACITANCE: (P6,P5,P4) TO (J6,J3)  
   (P3,P2,P1) TO (J2,J1)  
   : 30pf MAX. @ 1MHz

5.0 DC RESISTANCE: (J6–J3) = (J2–J1)  
   : 1.2 ohms Max.

NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

REV.: PA   PAGE: 2
6.0 RETURN LOSS: 1MHz TO 30MHz
   60MHz TO 80MHz
   : 18dB MIN.
   : 12dB MIN.

   NOTE: 100 OHMS CONNECTED TO (J2–J1) OR (J6–J3).

7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P3)
   (J3, J6) TO (P4, P6)
   : 1500 VAC

8.0 INSERTION LOSS: RS=RL=100 ohms
   100kHz TO 100MHz
   : 1.1 dB TYP

9.0 RISE TIME: RS=100 OHMS AND RL = 100 OHMS
   OUTPUT VOLTAGE = 1 V peak
   PULSE WIDTH= 112nS
   : 3.0 nS MAX
   : 3.0 nS MAX

10.0 CROSS TALK: 1MHz TO 100MHz
   : 40 dB TYP

11.0 COMMON TO COMMON MODE ATTENUATION: 30MHz TO 100MHz
   : 35dB TYP
0.530 [13.46]
0.050 [1.27] (7)
0.050 [1.27]
0.080 [2.03]

Ø0.035±0.003 [Ø0.89±0.08] (7)
Ø0.062±0.003 [Ø1.57±0.08] (2)
Ø0.128±0.003 [Ø3.25±0.08] (2)

PCB Recommended Hole Layout
(Seen from Component Side)

All centerline dimensions are basic.
SUGGESTED PANEL OPENING

NOTES:
THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.