ELECTRICAL CHARACTERISTICS @ 25°C

1.0 TURNS RATIO: (P4-P5-P6) : (J3-J6) : 1CT : 1CT ± 3%
(P3-P2-P1) : (J2-J1) : 1CT : 1CT ± 3%

2.0 INDUCTANCE:  
(P4-P6) : 350uH MIN. @ 0.1V, 100kHz, 8mA DC Bias
(P3-P1) : 350uH MIN. @ 0.1V, 100kHz, 8mA DC Bias

3.0 LEAKAGE INDUCTANCE: P6-P4 (WITH J6 AND J3 SHORT) : 0.3uH MAX. @ 1MHz
P3-P1 (WITH J2 AND J1 SHORT) : 0.3uH MAX. @ 1MHz

4.0 INTERWINDING CAPACITANCE: (P6,P5,P4) TO (J6,J3): 30pF MAX @ 1MHz
(P3,P2,P1) TO (J2,J1): 30pF MAX. @ 1MHz

5.0 DC RESISTANCE: (J6-J3)=(J2-J1) : 1.35 ohms Max.

6.0 RETURN LOSS:(P4-P6)=100 OHMS AND (P1-P3)=100 OHM REF.
1MHz TO 30MHz : 18dB MIN.
60MHz TO 80MHz : 12dB MIN.
NOTE: 100 OHMS CONNECTED TO (J2-J1) OR (J3-J6).

7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P3) : 1500 Vrms
(J3, J6) TO (P4, P6) : 1500 Vrms

8.0 INSERTION LOSS: RS=RL=100 ohms
100kHz TO 100MHz : 1.1 dB TYP

9.0 RISE TIME: RS=100 OHMS AND RL = 100 OHMS
OUTPUT VOLTAGE = 1 V peak
PULSE WIDTH= 112ns
: 3.0 nS MAX
: 3.0 nS MAX

10.0 CROSS TALK: 1-100 MHz
: 40 dB TYP

11.0 COMMON TO COMMON MODE ATTENUATION: 30MHz TO 100MHz : 35dB TYP

NOTES: 1.0 UNUSED PIN P7 IS OMITTED.
NOTES:

1. CONNECTOR MATERIALS:
   - HOUSING: THERMOPLASTIC UL94 V-0
   - CONTACT/SHIELD: COPPER ALLOY
   - SHIELD PLATING: NICKEL OR TIN
   - CONTACT PLATING: 50 MICRO-INCH SELECTIVE HARD GOLD PLATING
     OR EQUIVALENT IN CONTACT AREA

2. PIN NOT ELECTRICALLY CONNECTED MAY BE OMITTED.
   SEE ELECTRICAL DRAWING FOR OMITTED PINS.

3. TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.

4. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ±0.005 [0.13]

5. THE PRODUCT IS RoHS COMPLIANT.

6. THE PART IS RECOMMENDED FOR WAVE SOLDERING.
   THE SUGGESTED PEAK WAVE SOLDERING CONDITION IS
   260°C MAX AND 10 SECONDS MAX.

**FILE NAME**
SI-50170-F_B.DWG

**DATE**
2018-01-31

**DRAWN BY**
LIU DONGJUN

**ORIGINATED BY**
ANTON LIAO

**PART NO. / DRAWING NO.**
SI-50170-F

**REV. : ** B

**PAGE : ** 3

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## LED Specification

<table>
<thead>
<tr>
<th>Color</th>
<th>Wavelength</th>
<th>Forward V (Max)</th>
<th>*(Typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Green</td>
<td>565 nm</td>
<td>2.5 V</td>
<td>2.2 V</td>
</tr>
</tbody>
</table>

*With a forward current of 20 mA (Typ)*

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### PCB Recommended HOLE LAYOUT

**seen from component side**

**all centerline dimensions are basic**

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**Originated by**: Anton Liad  
**Date**: 2018-01-31

**Drawn by**: Liu Dongjun  
**Date**: 2018-01-31

**Part No. / Drawing No.**: SI-50170-F

**File Name**: SI-50170-F_B.DWG

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The suggested panel opening is intended to give the user the ability to have reasonable jack/panel clearances yet maintain reliable grounding capability.