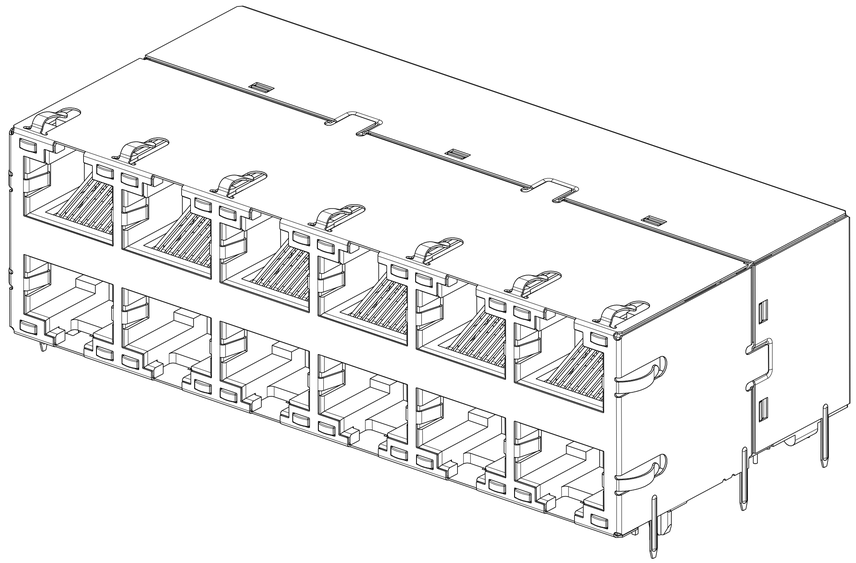
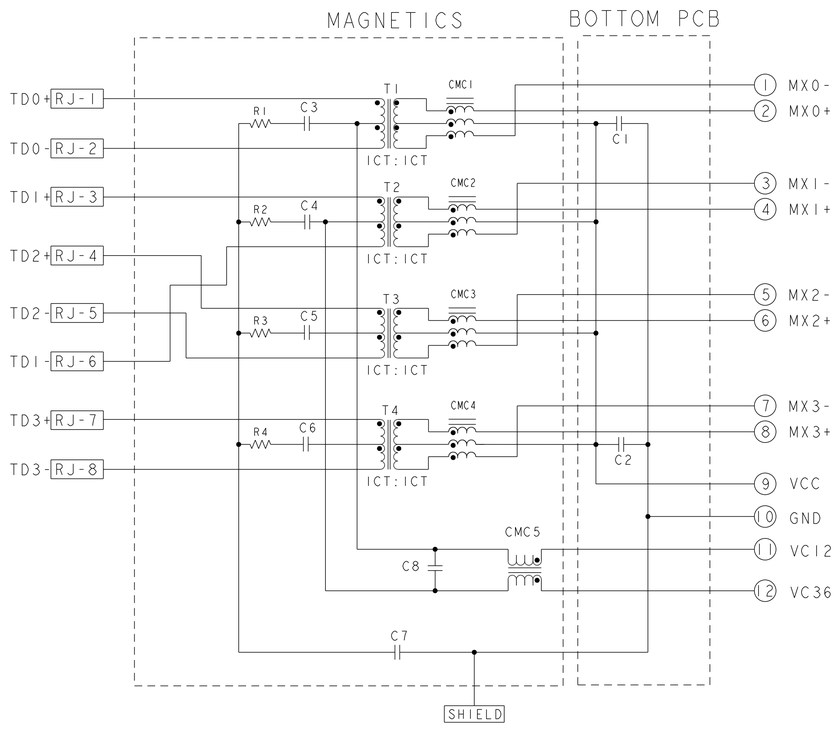
PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:
5736910 5939955 6425781 6428361 6554638 6840817 7123117
7429195 7717749 7808751 8217391 8149050 7924130

REVISIONS					
P	LTR	DESCRIPTION	DATE	DWN	APVD
	D	LOGO CHANGE	16APR2013	RL	KZ
	E	EC-1412014 AND EC-1411035 LOGO CHANGE	11DEC2014	TR	TY



S9HG02C2 GIGABIT PoE PLUS CIRCUIT 2 7

TOP AND BOTTOM PORTS



C1-C2=10nF, 50V, CAPACITORS
C3-C6=22nF, 100V,CAPACITORS
C7=1000pF,2kV,CAPACITOR
C8=100nF,100V,CAPACITOR
R1-R4=75 OHMS,1/16W,RESISTORS

1. MATERIALS:
   PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0
   SHIELD: BRASS, PREPLATED WITH 0.76um MIN SEMI-BRIGHT NICKEL, POST DIPPED WITH 2.54um MIN SAC SOLDER ON SOLDER TAILS.
   CONTACTS: PHOSPHOR BRONZE, 1.27um MIN OVERALL NICKEL UNDERPLATE WITH 1.27um MIN GOLD OR WITH SELECT 0.05um MIN GOLD OVER 0.76um MIN PALLADIUM-NICKEL AT MATING INTERFACE AND 2.54um MIN MATTE TIN ON SOLDER TAILS.
   LED: DIFFUSED EPOXY LENS, CARBON STEEL LEAD FRAME TAILS OF LED ARE PREPLATED WITH 2.03um MIN SILVER OVER 1.02um MIN NICKEL UNDERPLATE OVER 1.02um MIN COPPER UNDERPLATE. POST-PLATED WITH 2.54um MIN MATTE TIN AND/OR SAC SOLDER DIP OR PURE TIN SOLDER DIP

2 MAGNETICS:
   APPLICATION: 10/100/1000 BASE-T, PoE PLUS
   IMPEDANCE: 100 OHMS
   TURNS RATIO (CHIP:CABLE): 1:1 ALL FOUR PAIRS
   OPEN CIRCUIT INDUCTANCE (OCL):
   ALL CHANNELS 350 uH MIN @ 100KHz, 0.1 VRMS WITH 8mA DC BIAS FROM 0°C TO 70°C, 120 uH min @ 100KHz, 0.1 VRMS WITH 19 mA DC BIAS FROM 0°C TO 70°C, ACROSS RJ1-RJ2 & RJ3-RJ6.
   ALL FOUR PAIRS BI-DIRECTIONAL
   POE CURRENT: 600mA DC MAX
   PERFORMANCE @25°C:
   INSERTION LOSS (IL): 1.1dB MAX FROM 1.0MHz TO 100MHz
   RETURN LOSS (RL): 18dB MIN FROM 1.0MHz TO 40MHz
   12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz
   CROSSTALK ATTENUATION: 35dB MIN FROM 1.0MHz TO 40MHz
   33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz
   COMMON MODE REJECTION RATIO (CMRR):
   30dB MIN FROM 1.0MHz TO 100MHz
   ISOLATION VOLTAGE: 2250VDC(MAX) FOR 60 SECONDS WITH A RISE TIME OF 500V/SEC AND WITH ALL PORTS CONNECTED.

3 PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN LOCATED IN APPROXIMATE AREA SHOWN
DATE CODE: YYWWD WHERE "YY" IS YEAR, "WW" IS WORK WEEK, "D" IS DAY OF WEEK, WITH SUNDAY =1

4 TRP CONNECTOR LOGO AND AGENCY APPROVAL LOGO ARE LOCATED IN APPROXIMATE AREA SHOWN.

5. OPERATING TEMP: FROM 0°C TO 70°C.

6. RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.

7 INDICATED MAGNETIC CONNECTIONS ARE SYMMETRICAL AND SUPPORT AUTO-MDI/MDIX.

8 DATUM AND BASIC DIMENSION ESTABLISHED BY CUSTOMER.

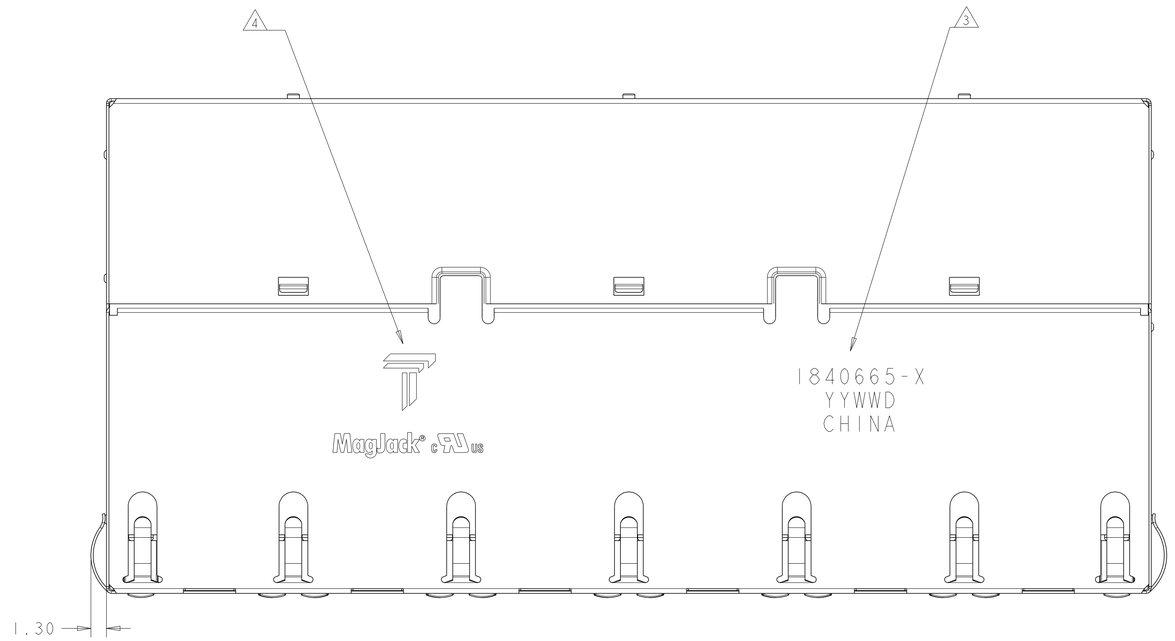
9 DIMENSION ESTABLISHED BY CUSTOMER, BUT MAY NOT BE GREATER THAN 5.08mm.

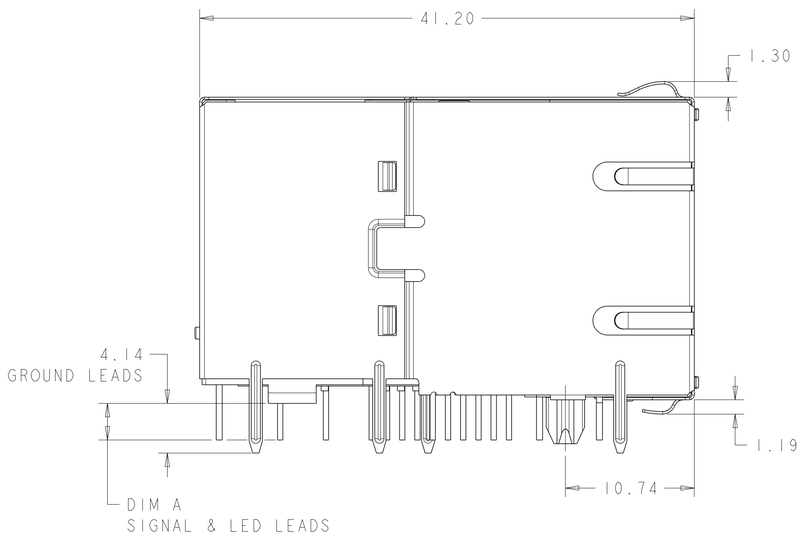
10 LEDS ARE DRIVEN WITH CONSTANT CURRENT AT APPROX 20mA
LED COLOR: DOMINANT WAVELENGTH (λD): GREEN 568 nm TYP. @ IF=20mA
FORWARD VOLTAGE (VF): GREEN 2.2V TYP. @ IF=20mA
DOMINANT WAVELENGTH (λD): YELLOW 588 nm TYP. @ IF=20mA
FORWARD VOLTAGE (VF): YELLOW 2.1V TYP. @ IF=20mA

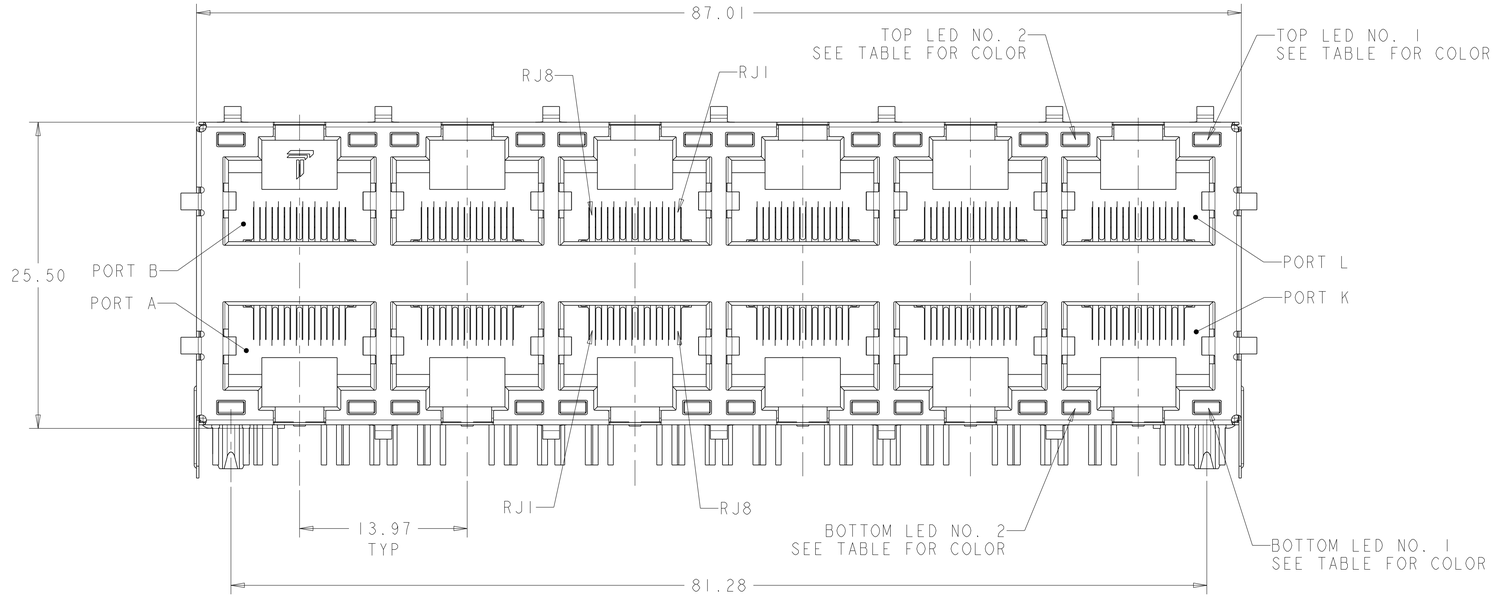
11. THESE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS, PEAK TEMPERATURE 260°C FOR 10 SECONDS

2.60	GREEN/YELLOW	GREEN/YELLOW	GREEN/YELLOW	GREEN/YELLOW	1840665-2
3.04	GREEN/YELLOW	GREEN/YELLOW	GREEN/YELLOW	GREEN/YELLOW	1840665-1
DIM A	BOTTOM LED NO. 2	BOTTOM LED NO. 1	TOP LED NO. 2	TOP LED NO. 1	PART NO.

THIS DRAWING IS A CONTROLLED DOCUMENT.
DIMENSIONS: mm
TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ±0.25, 1 PLC ±0.25, 2 PLC ±0.25, 3 PLC ±-, 4 PLC ±-, ANGLES ±-
PRODUCT SPEC 108-104004
APPLICATION SPEC -
DWN 03NOV2011 RICK LI/EVAN MA
CHK 03NOV2011 TONY YUAN
APVD 23OCT2013 KEITH ZHU
trp CONNECTOR a bel group DONGGUAN CHINA
MODEL NAME MAGJACK STACK PoE+
DESC 2X6 S9HG02C2 GIGABIT PoE+ W/ LED
SIZE A1 | CAGE CODE | DRAWING NO C-1840665 | RESTRICTED TO -
CUSTOMER DRAWING | SCALE 4:1 | SHEET 1 OF 4 | REV E







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DIMENSIONS: mm

TOLERANCES UNLESS OTHERWISE SPECIFIED:
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1 PLC ±0.25
2 PLC ±0.25
3 PLC ±-
4 PLC ±-
ANGLES ±-

PRODUCT SPEC: 108-104004
APPLICATION SPEC: -

DWN 03NOV2011 RICK LI/EVAN MA
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APVD 23OCT2013 KEITH ZHU

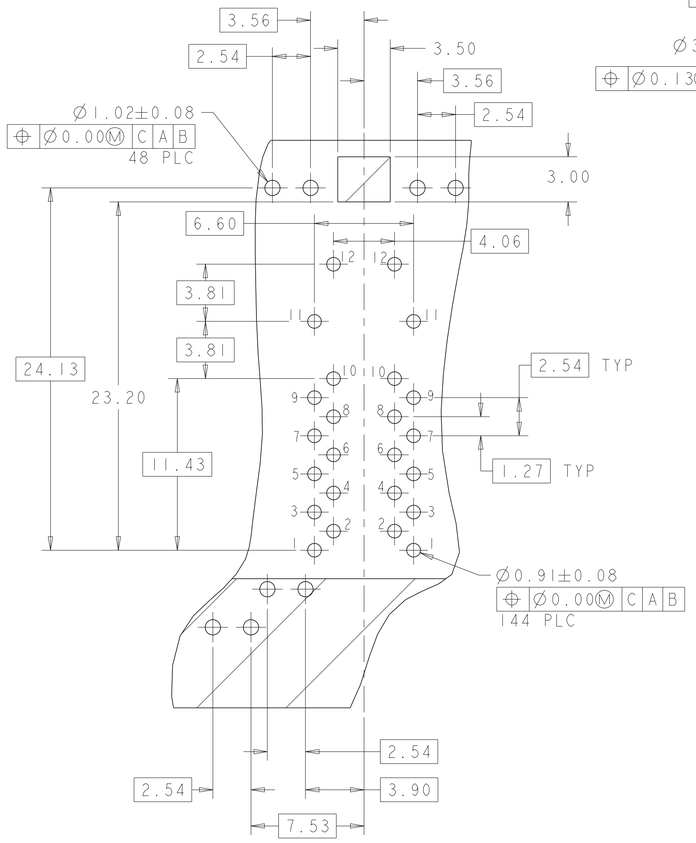
trp CONNECTOR a bel group — DONGGUAN CHINA

MODEL NAME: MAGJACK STACK PoE+

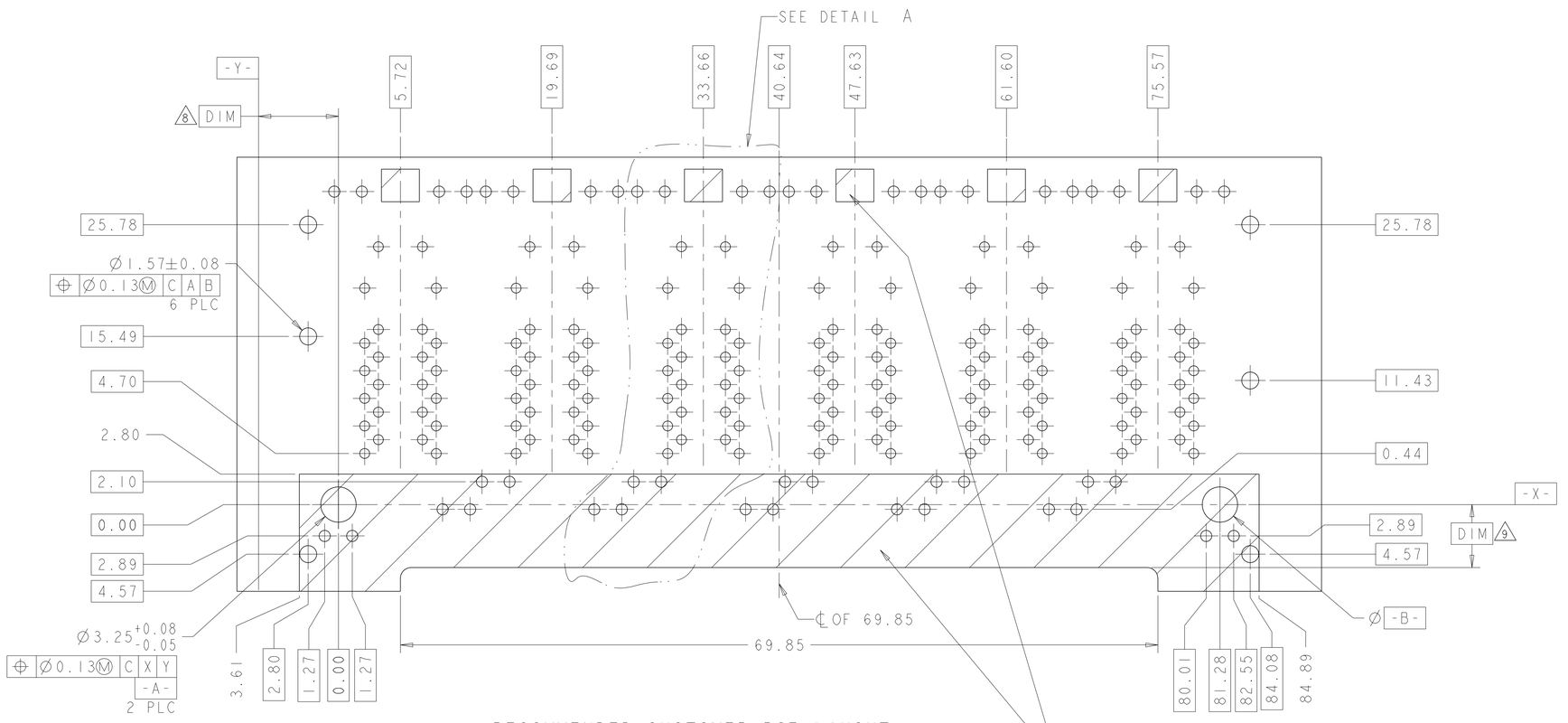
DESC: 2X6 S9HG02C2 GIGABIT PoE+ W/ LED

SIZE A1 | CAGE CODE | DRAWING NO C-1840665 | RESTRICTED TO -

CUSTOMER DRAWING | SCALE 4:1 | SHEET 2 OF 4 | REV E

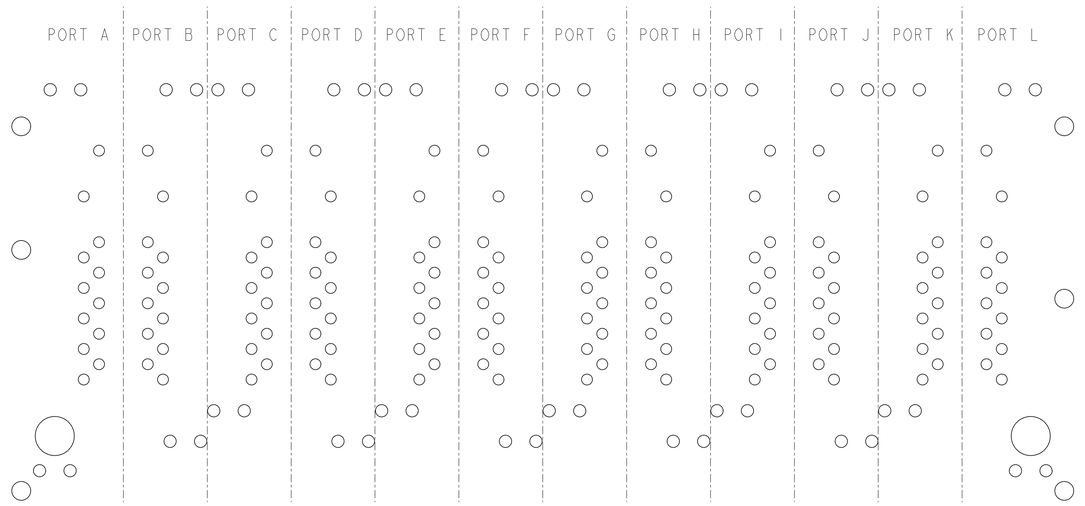


DETAIL A
SCALE 5:1



RECOMMENDED CUSTOMER PCB LAYOUT
VIEWED FROM COMPONENT SIDE

IT IS RECOMMENDED THAT SHADED AREAS ON CUSTOMER PC BOARD BE CLEAR OF ANY VIA HOLE, COMPONENT, CIRCUIT TRACE WHICH HAS EQUAL POTENTIAL WITH CABLE SIDE SIGNAL AND POE SIGNAL



PORT ASSIGNMENT
VIEWED FROM COMPONENT SIDE
SCALE 4:1

THIS DRAWING IS A CONTROLLED DOCUMENT.

DIMENSIONS: mm

TOLERANCES UNLESS OTHERWISE SPECIFIED:
0 PLC ±0.25
1 PLC ±0.25
2 PLC ±0.25
3 PLC ±-
4 PLC ±-
ANGLES ±-

PRODUCT SPEC: 108-104004
APPLICATION SPEC: -

DWN 03NOV2011 RICK LI/EVAN MA
CHK 03NOV2011 TONY YUAN
APVD 23OCT2013 KEITH ZHU

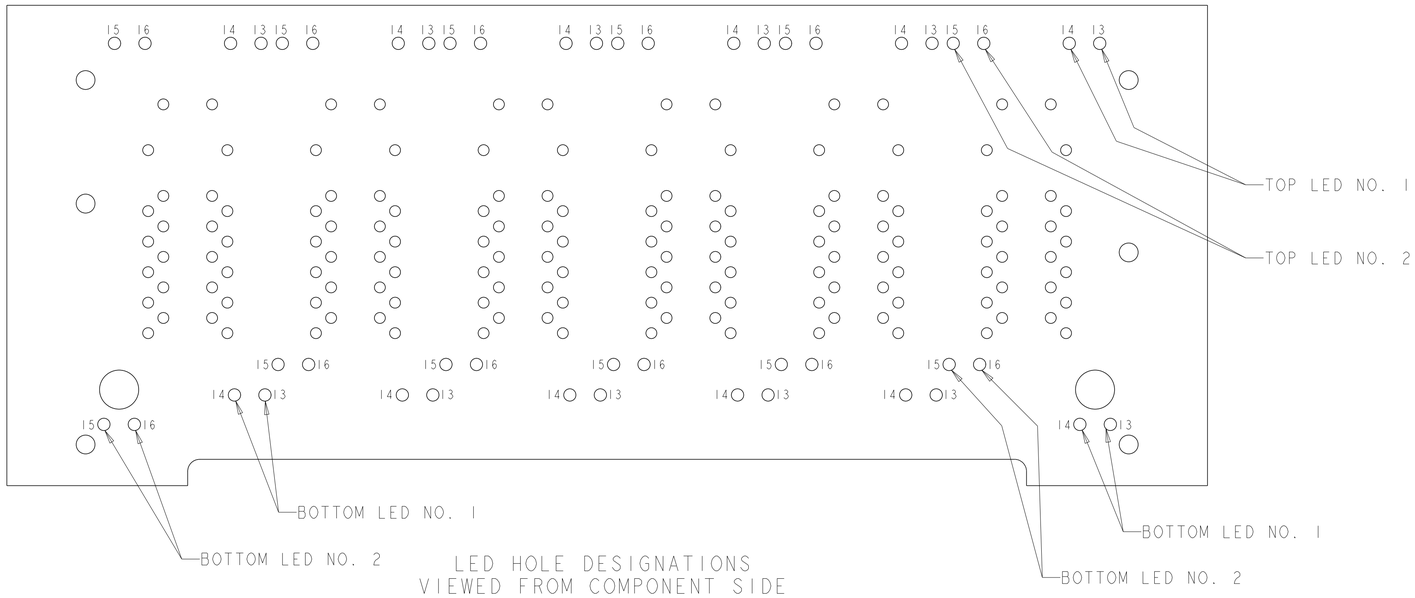
trp CONNECTOR a bel group
DONGGUAN CHINA

MODEL NAME: MAGJACK STACK PoE+

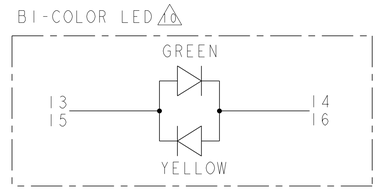
DESC: 2X6 S9HG02C2 GIGABIT PoE+ W/ LED

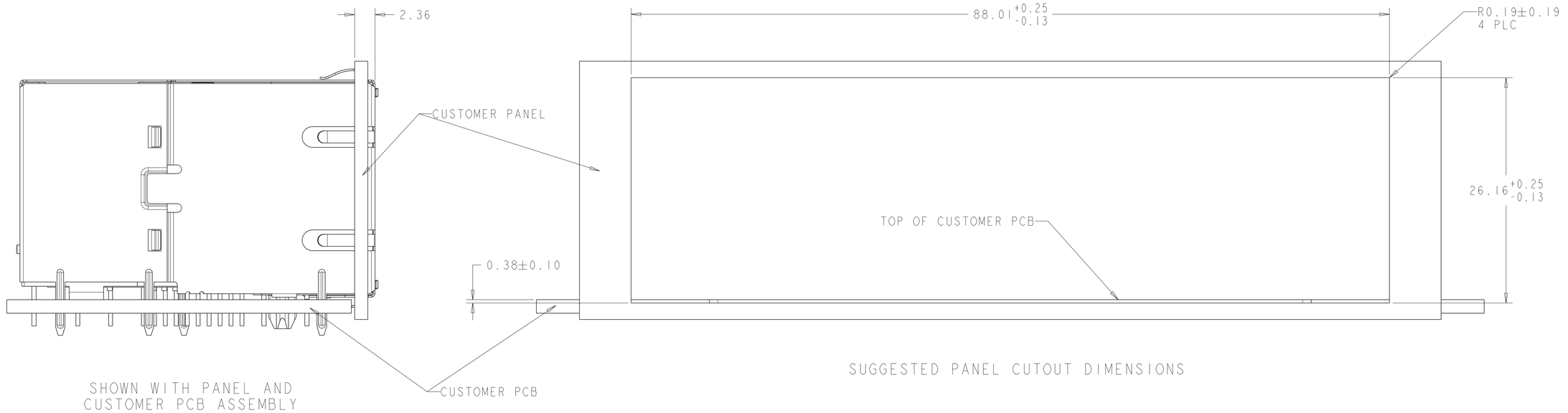
SIZE A1 | CAGE CODE | DRAWING NO C-1840665 | RESTRICTED TO -

CUSTOMER DRAWING | SCALE 4:1 | SHEET 3 OF 4 | REV E



LED HOLE DESIGNATIONS
VIEWED FROM COMPONENT SIDE
SCALE 4:1





SHOWN WITH PANEL AND
CUSTOMER PCB ASSEMBLY

SUGGESTED PANEL CUTOUT DIMENSIONS

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN 03NOV2011 RICK LI/EVAN MA	trp CONNECTOR a bel group — DONGGUAN CHINA
		CHK 03NOV2011 TONY YUAN	
DIMENSIONS: mm	TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ±0.25; 1 PLC ±0.25; 2 PLC ±0.25; 3 PLC ±-; 4 PLC ±-; ANGLES ±-	APVD 23OCT2013 KEITH ZHU	MODEL NAME: MAGJACK STACK PoE+
PRODUCT SPEC 108-104004	APPLICATION SPEC -		DESC: 2X6 S9HG02C2 GIGABIT PoE+ W/ LED
			SIZE A1 · CAGE CODE · DRAWING NO C-1840665 · RESTRICTED TO -
		CUSTOMER DRAWING	SCALE 4:1 · SHEET 4 OF 4 · REV E