PET800-12-074xA Series

AC-DC Front-End Power Supply

The PET800-12-074xA is an 800 Watts, 1 U form factor power supply module with Active PFC (Power Factor Correction) and Power Management Bus. It converts standard AC mains power into a main output of 12 V for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PET800-12-074xA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



Key Features & Benefits

- Best-in-Class, 80 PLUS Certified “Platinum” Efficiency
- Wide Input Voltage Range 90-264 VAC
- AC Input with Power Factor Correction
- Always-On 24 W Standby Output (12 V / 2 A)
- Hot-Plug Capable
- Parallel Operation with Active Digital Current Sharing
- DC-DC Digital Controls for Improved Performance
- High Density Design 25 W/in^3
- Small Form Factor 185 x 73.5 x 39 mm (7.28 x 2.89 x 1.53 in)
- Power Management Bus Communications Protocol for Control, Programming and Monitoring
- Over Temperature, Output Over Voltage and Over Current Protection
- One DC OK Signaling Status LED

Applications

- High Performance Servers
- Routers
- Network Switches

Please read our datasheet & drawing disclaimer here.

1. ORDERING INFORMATION

PET	800	-	12	-	074	x	A
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**
PET	800 W		12 V		74 mm	N: Normal R: Reversed	A: AC

2. OVERVIEW

The PET800-12-074 AC-DC power supply is a mainly DSP controlled, highly efficient front-end. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range, the PET800-12-074 maximizes power availability in demanding server, network switch, and router applications.

The front-end is fan cooled and ideally suited for server integration with a matching airflow path. The PFC stage is controlled using interleaved Critical mode to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant technology in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output, provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

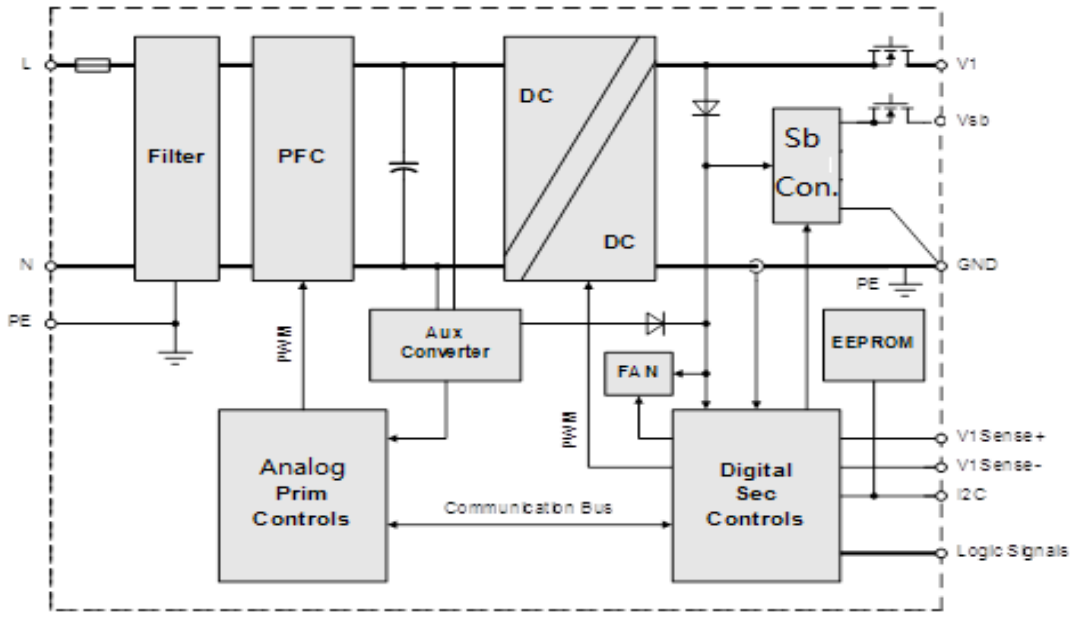


Figure 1. PET800-12-074 Block Diagram

3. INPUT

General Condition: TA = 0… 50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Input Voltage Ranges	Low line	90	115	132	VAC
		High line	180	230	264	VAC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90		264	VAC
$I_{i\,max}$	Max Input Current				12	A_{rms}
$I_{i\,p}$	Inrush Current Limitation[1] (Cold start)	$V_{i\,min}$ to $V_{i\,max}$, 90°(Phase), T_{NTC} = 25 °C			50	A_p
I_i	Input current	90-132 VAC			12	A_{rms}
		180-264 VAC			6	A_{rms}
F_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	Vi nom, 50 Hz, I1 nom	0.93			W/VA
$V_{i\,on}$	Turn-on Input Voltage	Brown in	80	85	90	VAC
$V_{i\,off}$	Turn-off Input Voltage	Brown out	75	80	85	VAC
η	Efficiency without Fan	$V_{i\,nom}$, 0.2·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		92		%
		$V_{i\,nom}$, 0.5·$I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		94.2		
		$V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		93		
T_{hold}	Hold-up Time	After last AC zero point		16		ms

3.1 EFFICIENCY

The power supply module efficiency should meet at least 80Plus Platinum rating, the efficiency should be measured at 230 VAC and with external fan power according to 80Plus efficiency measurement specifications.

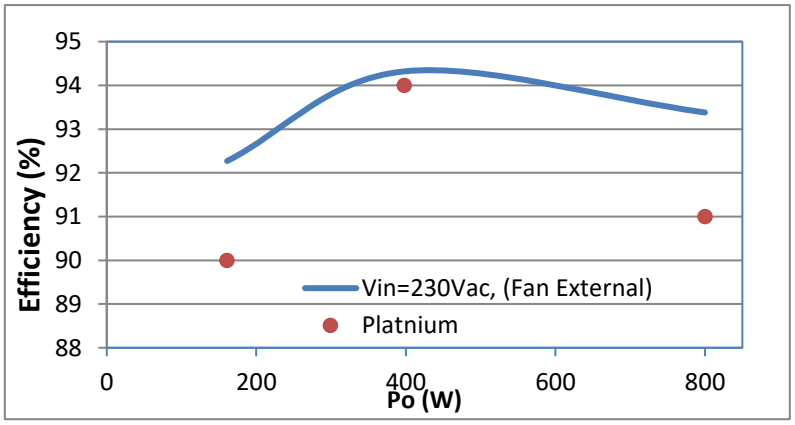


Figure 2. Efficiency vs. Load Current (Ratio Metric Loading)

[1] The charging currents for X capacitors are not considered as in-rush current

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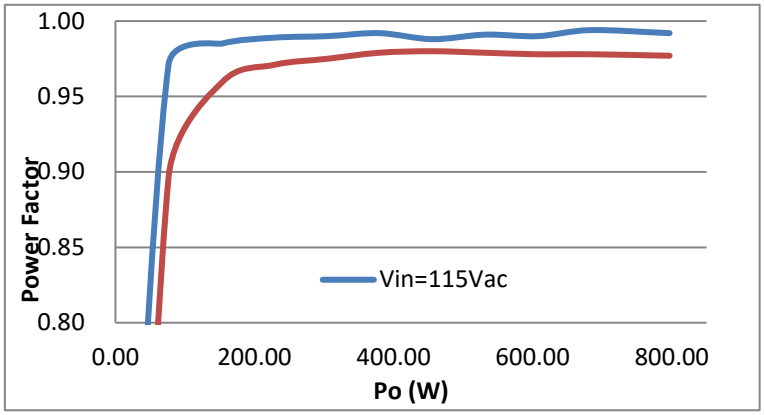


Figure 3. Power factor vs. Load current

4. OUTPUT

General Condition: Ta = 0 … +50 °C unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-0.5		+0.5	% $V_{1\ nom}$
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% V_{SBnom}
$P_{1\ nom}$	Nominal Output Power	V_1 = 12V		780		W
$I_{1\ nom}$	Nominal Output Current[2]	Input voltage 100-264 VAC Input voltage 900-100 VAC		65 59.6		ADC
$v_{1\ pp}$	Output Ripple Voltage[3]	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See Section 4.1)			120	mVpp
dI_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-6.5		+6.5	ADC
VI_{share}		$V_{1\ nom}$, I_1 =65A		6.0		VDC
dV_{dyn}	Dynamic Load Regulation	ΔI1 = 60% I1 nom, I1 = 5 … 100% I1 nom, dI1/dt = 0.5 A/µs, recovery within 1% of V1 nom	-5		+5	% $V_{1\ nom}$
T_{rec}	Recovery Time				2	ms
$C_{V1\ Load}$	Capacitive Loading	T_a = 25 °C			1,1000	µF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25 °C		12.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	% V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-5		+5	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power			24		W
$I_{SB\ nom}$	Nominal Output Current			2		ADC
$V_{SB\ pp}$	Output Ripple Voltage[3]	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW			120	mVpp
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 25% I_{SB} nom, I_{SB} = 5 … 100% I_{SB} nom, dI_{SB}/dt = 0.5 A/µS, recovery within 1% of V_{SB} nom	-5		+5	% V_{SBnom}
T_{rec}	Recovery Time				250	µs
$C_{VSB\ load}$	Capacitive Loading for V_{SB}	T_{amb} = 25 °C			350	µF

[2] The output noise and ripple measurement was made with 20 MHz bandwidth using a 6 inch twisted pair, terminated with a 10 uF tantalum capacitor in parallel with a 0.1 uF ceramic capacitor. The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.
[3] The output power derating at low line only for PET800-12-050NA, for RA model no derating required

4.1 GROUNDING

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC-current.

4.2 HOT SWAP REQUIREMEENTS

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON asserted, while in standby mode with PSON de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON asserted, with PSON de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general, a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

5. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (Line)	Not user accessible, quick-acting (F)		12.5		A_{rms}
$V_{1\ OV}$	OV Threshold V_1	Refer to section 5.1	13.3		14.5	VDC
$V_{1\ UV}$	UV Threshold V_1	unlatch unit by disconnecting AC or by toggling the PS_ON signal		10.5		VDC
$I_{V1\ lim}$	Current Limit V_1	Refer to section 5.3	71.5		97.5	ADC
$I_{V1\ SC}$	Max Short Circuit Current V_1	V1 < 3 V (unlatch unit by disconnecting AC or by toggling the PS_ON signal)		250		ADC
$V_{SB\ OV}$	OV Threshold V_{SB}	unlatch unit by disconnecting AC	13.3		14.5	VDC
$I_{SB\ lim}$	Current Limit V_{SB}	Hiccup mode	3.5		4.5	ADC
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis_for NA model		70		°C
	Over Temperature Oring	Automatic recovery with Hysteresis_for NA model		100		°C
T_{SD}	Over Temperature on Inlet	Automatic recovery with Hysteresis_ for RA model		60		°C
	Over Temperature Oring	Automatic recovery with Hysteresis_ for RA model		105		°C

5.1 OVER VOLTAGE PROTECTION

The PET front-ends provide a fixed threshold over voltage protection implemented with a HW comparator. Once an over voltage condition has been triggered, the power supply will shut down and latch the fault condition. The latch can be unlatched by disconnecting the supply from the AC mains or by toggling the PS_ON input.

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5.2 UNDER VOLTAGE PROTECTION

The main output will latch off when V1 drop to below the UV threshold. The latch can be unlatched by disconnecting the supply from the AC mains or by toggling the PS_ON input. The main output will shut down if the VSB voltage drop below 8V and recover when VSB voltage higher than 10 V.

5.3 CURRENT LIMITATION

Main Output

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~10.8 VDC for more than 10 ms, the output will latch off (standby remains on).

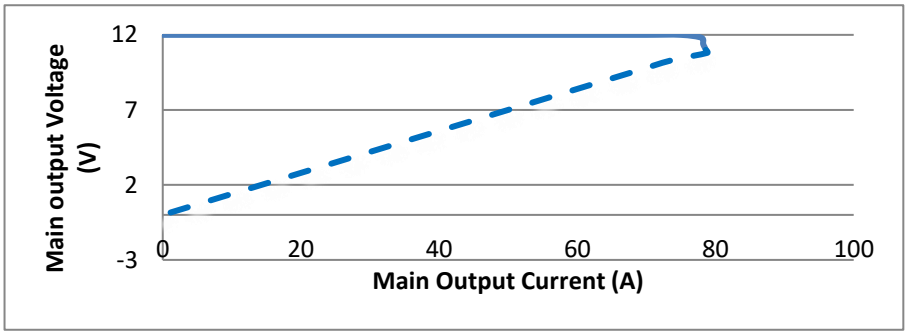


Figure 4. Current Limitation on V1 (Vi = 230 VAC)

A second current limitation circuit on V1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PS_ON input.

Standby Output

The standby output exhibits a substantially rectangular output characteristic down to 0 V (hiccup mode). If it runs in current Limitation and standby output will be shut down and power supply into hick up mode, the main output will be inhibited during the status.

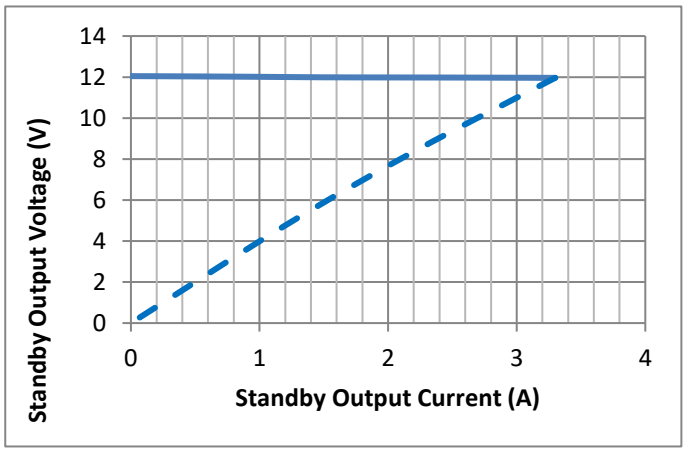


Figure 5. Current limitation on VSB

6. TIMING SPECIFICATIONS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 70 ms. For 12 VSB, it is allowed to rise from 1 to 25 ms. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

6.1 OUTPUT VOLTAGE TIMING

The timing of signals and outputs are specified in the Table below and illustrated in Figure 6.

ITEM	DESCRIPTION	MIN	MAX	UNITS
Tvout_rise	Output voltage rise time from each main output		70	ms
Tsb_on-delay	Delay from AC being applied to 12VSB being within regulation.		1500	ms
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all main output 12VI voltage stay within regulation after loss of AC.	16		ms
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK.	12		ms
Tpson_on_delay	Delay from PSON# active to output voltage within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.		50	ms
Tpwok_on	Delay from output voltage (12V) within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok_off	Delay from PWOK de-asserted to output voltage dropping out of regulation limits.	4		ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 12VSB being in regulation to main output being in regulation at AC turn on.	50	1000	ms
TVSB_holdup	Time the 12VSB output voltage stays within regulation after loss of AC	70		ms

Table 1. Turn on/off timing

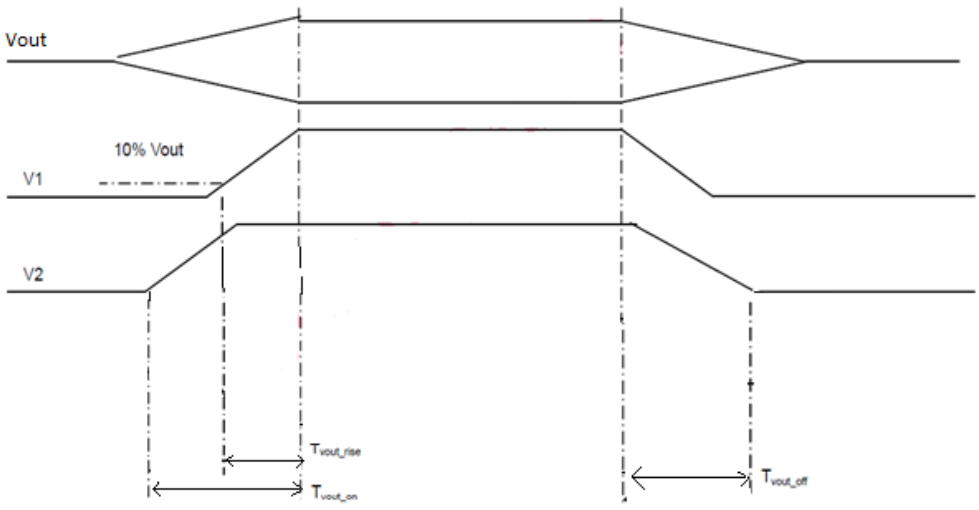


Figure 6. Output Voltage timing

Tvout_rise: The 12 Vsb and 12 V output rise time shall be 1 ms to 25 ms.

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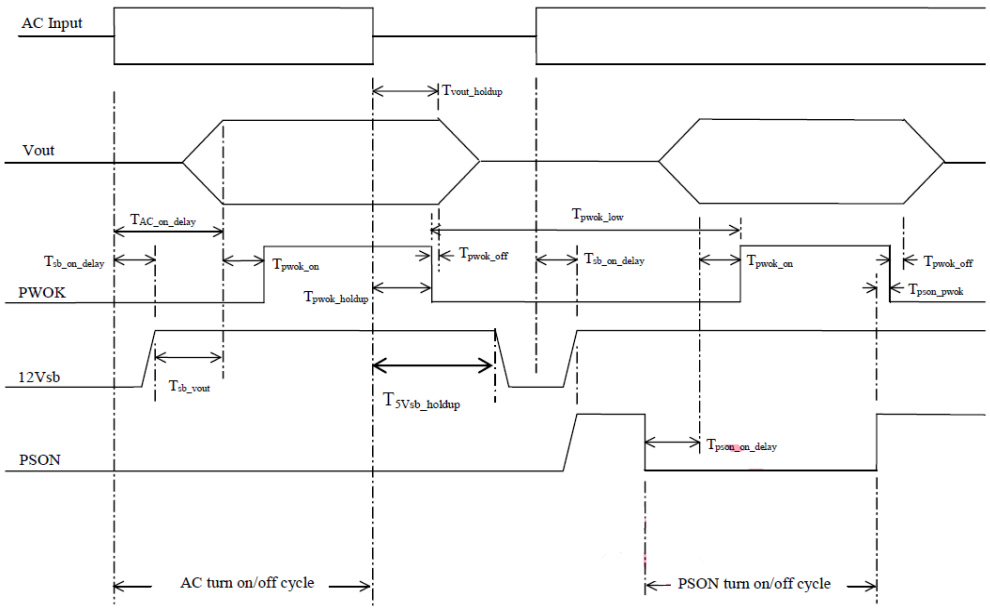


Figure 7. Turn On/Off Timing

6.2 OVER SHOOT

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 10 ms.

6.3 UNDER SHOOT

Any output shall not undershoot at turn on or off cycle under any circumstances.

6.4 TEMPERATURE COEFFICIENT

After operating for 30 minutes or longer at 25 ° C ambient, the output voltages shall not change by more than ±0.05% per degree C for any given line and load conditions.

7. MONITORING FOR POWER MANAGEMENT BUS ACCURACY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{I\ mon}$	Input RMS Voltage	$V_{I\ min} \le V_I \le V_{I\ max}$	-3		+3	%
$I_{I\ mon}$	Input RMS Current	$I_I > 4\ A_{rms}$	-10		+10	%
		$I_I \le 4\ A_{rms}$	-0.4		+0.4	A_{rms}
$P_{I\ mon}$	True Input Power	$P_I > 200$ W	-10		+10	%
		$P_I \le 200$ W	-20		+20	W
$V_{1\ mon}$	V_1 Voltage		-2		+2	%
$I_{1\ mon}$	V_1 Current	I1 > 10 A	-3		+3	%
		I1 ≤ 10 A	-0.3		+0.3	A
$P_{o\ nom}$	Total Output Power	Po > 200 W	-5		+5	%
		Po ≤ 200 W	-10		+10	W
$V_{SB\ mon}$	Standby Voltage		-2		+2	%
$I_{SB\ mon}$	Standby Current	$I_{SB} \le I_{SB\ nom}$	-0.2		+0.2	A

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PS ON# Signal Characteristics					
Signal type (Active Low)	Accepts an open collector/drain input from the system. Pul-up to Vsb located in the power supply.				
PSON = Low	ON				
PSON= Open or High	OFF				
PSON = Low	OFF				
Logic level low	Power supply ON	0		1.0	V
Logic level high	Power supply OFF	2.0		5.25	V
Source current	Vpson = low			4	mA
Power up delay	T pson on delay	5		400	ms
PWOK delay	T pson pwok			50	ms
PWOK Signal Characteristics					
Signal type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
PWOK = High	Power Good				
PWOK = Low	Power Not Good				
Logic level low voltage	Isink = 4 mA	0		0.4	V
Logical level high voltage	Isource = 200 uA	2.4		5.25	V
Sink current	PWOK = low			4	mA
Source current,	PWOK = high			2	mA
PWOK delay	Tpwok on	100		500	ms
PWOK rise and fall time				100	µs
Power down delay	Tpwok off	1		200	ms
SMB Alert Signal Characteristics					
Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
Alert = High	Power OK				
Alert = Low	Power Alert to system				
Logic level low voltage	Isink = 4 mA	0		0.4	V
Logic level high voltage	Isink = 50 µA	2.4		3.46	V
Sink current	Alert = low	-		4	mA
Sink current	Alert = high			50	µA

NOTE: Signals that can be defined as low true use the following convention: Signal = low true

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.
If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in *Figure 7* (except for SMB_ALERT, PW_OK pins). This will ensure the pin voltage is not affected by an unpowered power supply.

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8.3 FRONT LEDS

Status information is indicated by front-panel LED, LED is bi-colored: green and yellow.
See Table for different LED status.

POWER SUPPLY CONDITION	LED
No AC power to all PSU	OFF
AC present/only standby output on	1 Hz Flashing Green
Power supply DC output ON and OK	Green
Power supply failure	Yellow
Power supply warning	0.5 Hz Flashing Yellow*/Green*

NOTE: * Flashing frequency: 1 Hz (0.5 sec Yellow/ 0.5 sec Green)

8.4 PS_ON

The PS_ON signal is required to remotely turn on/off the main output of the power supply. PS_ON is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PS_ON is pulled to a standby voltage by a pull-up resistor internal to the power supply.

8.5 PWOK

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

8.6 SMB ALERT

The SMB_ALERT is an output signal and it is pulled to 3.3 V by a 4.7 K resistor in power supply. This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

8.6.1 THERMAL CLST

SMB Alert shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST shall assert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching below specified _T to critical shut down. The power supply shall report the temperature in addition to Thermal CLST through.

8.7 PDB_ALERT

To receive ALERT signal from system or PSU backplane, If signal is pulled LOW, the PSU internal fan shall be forced to run at maximum speed to improve thermal performance.

8.8 PDB-FAULT

To receive a FAULT signal from system or PSU backplane. PSU shall shutdown if this pin is pulled HIGH.

8.9 CURRENT SHARE

All outputs shall be capable of operating in a redundant current share mode. Eight power supplies may be operated in parallel. All outputs shall incorporate an isolation diode for fault isolation. Filter capacitors that are located after the isolation diode shall be of high reliability and shall be de-rated sufficiently to minimize failures. The +12 V current sharing

shall be a single wire type. Connecting the ISHARE pins of each power supply together shall enable the current share feature. With the current share pins tied together, the output load current shall be balanced as defined below. The load share (ISHARE) shall be a single wire type. Connecting ISHARE pins of each PCM together shall enable the current share feature. With the current share pins tied together, the output load current shall be balanced to within 10% of full load (current difference should be less than 6.5 A). Shorting or opening of a current share pin shall not cause the output voltage to go out of steady state regulation. For 65 A the ISHARE voltage shall be 6 V for a single power supply.

8.10 REMOTE SENSE

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 200 mV on the output return rail.

8.11 I²C / POWER MANAGEMENT BUS COMMUNICATION

The interface driver in the PET supply is referenced to the V1 Return. The PET supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and further characterized referenced in the Figure 8:

- There are 10K internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms

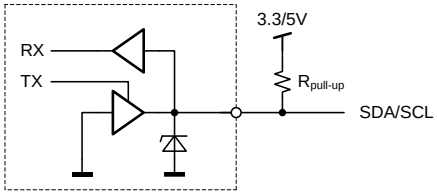


Figure 8. Physical layer of communication interface

The SMB_ALERT signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit).

PARAMETER		DESCRIPTION /CONDITION	MIN	MAX	UNIT
t_r	Rise time for SDA and SCL			1000	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF		300	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		mS

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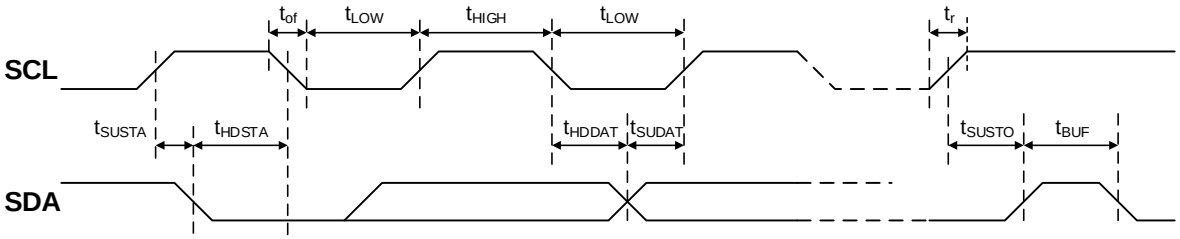


Figure 9. I²C / SMBus Timing

8.12 ADDRESS SELECTION

A1	A0	EEPROM ADDRESS	UNIT ADDRESS
0	0	0xA0	0xB0
0	1	0xA2	0xB2
1	0	0xA4	0xB4
1	1	0xA6	0xB6

8.13 CONTROLLER AND EEPROM ACCES

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 10). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 2K bytes of user memory. None of the bytes are used for the operation of the power supply.

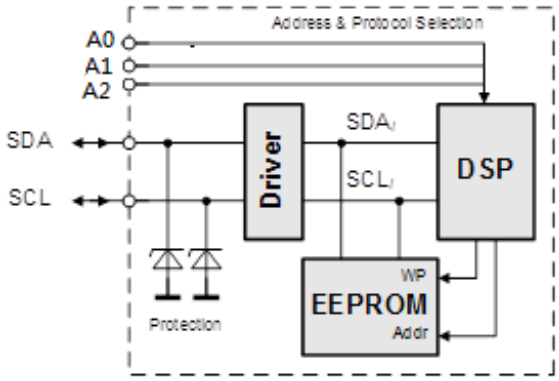


Figure 10. I2C Bus to DSP and EEPROM

8.14 EEPROM PROTOCOL

The EEPROM behaviour the same as the 24C02 series 8 bit address protocol. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

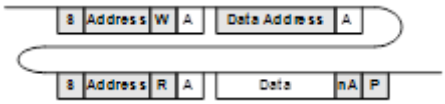
WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.15 POWER MANAGEMENT BUS PROTOCOL

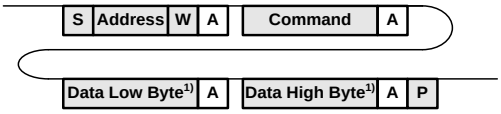
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PET800-12-074 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of > 25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

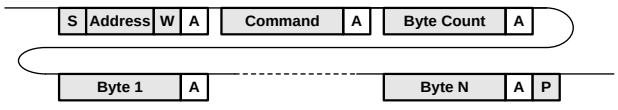
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



1) Optional

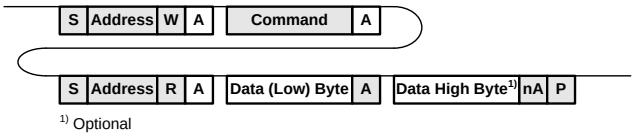
In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET800-12-074 Programming Manual for further information.



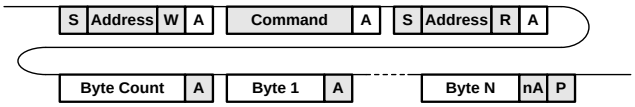
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READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PET800-12-074 Programming Manual for further information.



8.16 GRAPHICAL USER INTERFACE

Bel Power Solutions provide with its “Bel power solutions I2C” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET800-12-074 Front-End. The utility can be downloaded on: www.belpowersolutions.com and supports both the PSMI and Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PET800-12-074 Evaluation Kit it is also possible to control the PS_ON pin(s) of the power supply.

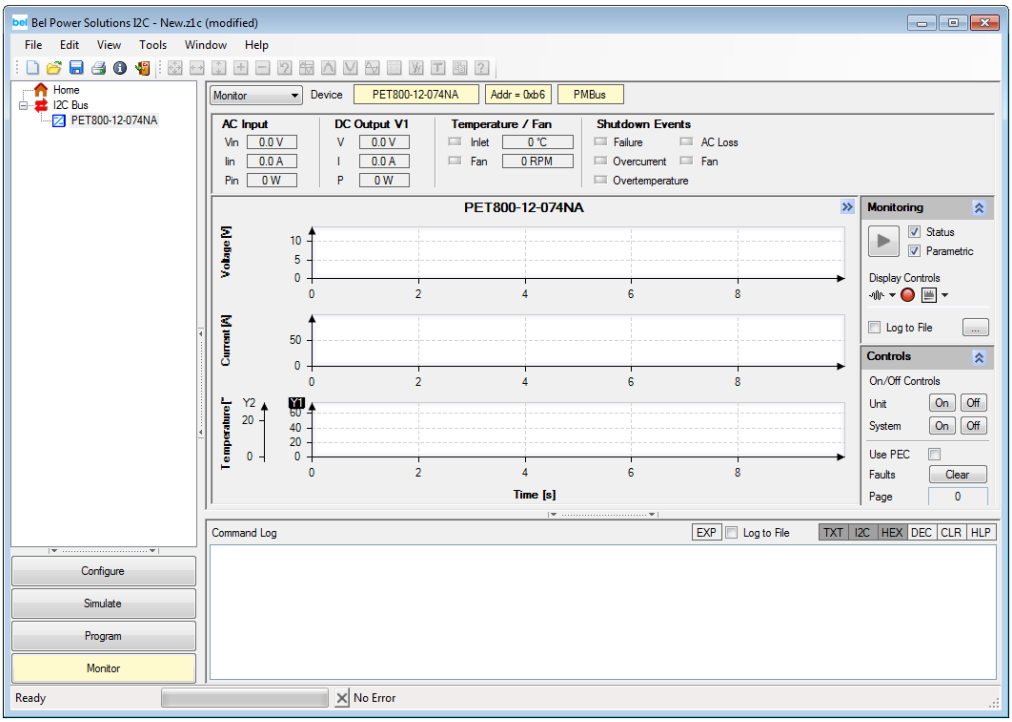


Figure 11. Monitoring dialog of the I2C Utility

9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET800-12-074 is provided with a normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.
For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.
The IEC connector on the unit is rated 100 °C. If 70 °C mating connector is used then end user must derate the input power to meet a maximum 70 °C temperature at the front, the rated output power should be 740 W if input voltage less than 100 VAC for PET800-12-074NA. don't need derate for PET800-12-074RA.

NOTE: It is the responsibility of the user to check the front temperature in such case. The unit will not limit its power automatically to meet such a temperature limitation.

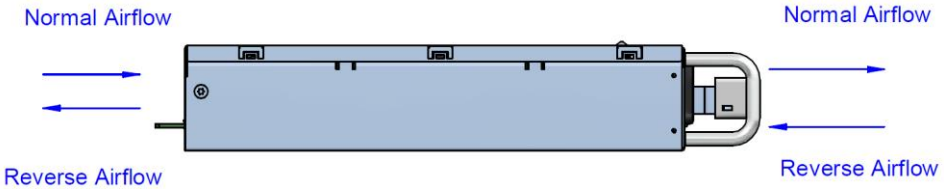


Figure 12. Airflow direction

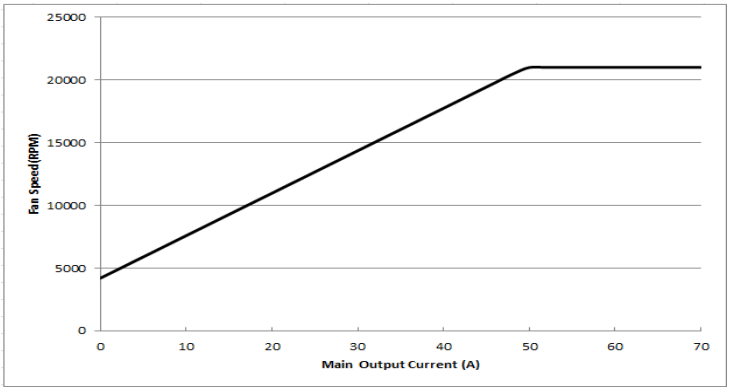


Figure 13. Fan speed vs. main output load

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10. ELECTROMAGNETIC COMPATIBILITY

PARAMETER	DESCRIPTION / CONDITION		CRITERION
Electromagnetic Interference	FCC / ICES-003 Emission (USA/Canada) Verification, CRISP 22 – Emission (International) , EN55022 – Emission (Europe), EN55024 – Immunity (Europe)		Class B
Harmonics	IEC61000-3-2		A
Flicker	IEC61000-3-3		
ESD Susceptibility	EN61000-4-2 Electrostatic Discharge: ± 8 KV contact discharge, ±15 KV Air discharge.		B
Radiated Susceptibility	EN61000-4-3 Radiated RFI Immunity: 10 V/m		A
EFT/Burst	EN61000-4-4 Electrical Fast Transients: Level 3		B
Surge Voltage	EN61000-4-5 Electrical Surge: CM; 2 KV, DM: 1 KV		B
Conducted Susceptibility	EN61000-4-6 RF Conducted: 10 V RMS		A
Power Frequency Magnetic Field Immunity	EN61000-4-8, 30 A/m		A
Voltage Dips and Interruptions	EN61000-4-11	30%(Voltage Dips), 10 ms	B
		60%(Voltage Dips), 100 ms	C
		>95%(Voltage Dips), 500 ms	C
Leakage Current	EN62368-1, 3.5 mA@264 VAC/60 Hz		

11. SAFETY/APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1 and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Agency Approvals	Approved to the latest revision/amendment of the following standards: • IEC 62368-1 • EN 62368-1 • UL/CSA 62368-1 • GB4943.1, GB9254.1; GB17625.1 • CNS15598-1, CNS15936		Approved by independent body (see CE Declaration)		
	CMTBF	The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25 °C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.				
	Isolation	Input to case (PE)		Basic		
		Input (L/N) to output		Reinforced		
dc	Creepage / Clearance	Primary to protective earth (PE)		3.0 minimum		mm
		Primary to secondary		6.0 minimum		
	Electrical Strength Test	Input to case	2500			VDC
		Input to output	4000			VDC

12. ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Temperature	Operating ambient temperature, normal mode (inlet air): Ta min to Ta max	0		+50	°C
	Operating, $T_{OP,}$ standby mode	-5		+50	°C
	Non-operating Ambient_ for NA model	-40		70	°C
	Non-operating Ambient_ for RA model	-40		60	°C
Humidity	Operating (Non-condensing)	10		85	%
	Non-operating (Non-condensing)	5		95	%
Altitude	Operating, above Sea Level	0		5000	m
	Non-operating, above Sea Level	0		15000	m
Mechanical Shock	A) Operation: 10 G, no malfunction B) Non-Operation: 50 G Trapezoidal Wave, Velocity change = 4.3 m/sec. Three drops in each of six directions are applied to each of the samples.				
Vibration	A) Operation: 0.01 g2/Hz at 10Hz, 0.02 g2/Hz at 20 Hz. B) Non-Operation: - **Sine sweep**: 5 Hz to 500 Hz @ 0.5 gRMS at 0.5 octave/min dwell 15min at each of 3 resonant points; - **Random profile**: 5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02g2 (slope up): 20 Hz to 500Hz @ 0.02 g2/Hz (flat); Input acceleration = 3.13 gRMS; 10 min. per axis for 3 axis on all samples				
Acoustic Noise	1 meter, 25 °C, 50% load		46		dBA

13. MECHANICAL PARAMETERS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		73.5		mm
	Height		39		
	Depth		185		
Weight			798		g

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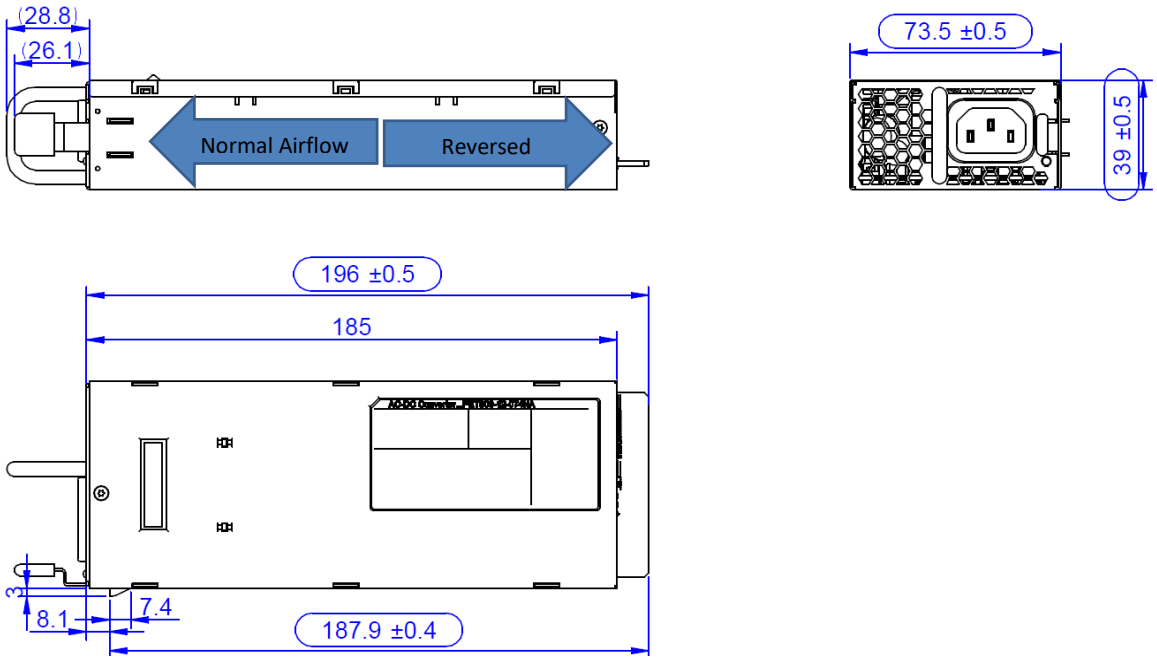


Figure 14. Mechanical Drawing-Side/Top View

NOTE: A 3D step file of the power supply casing is available on request.

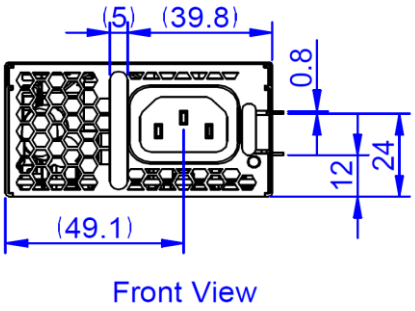


Figure 15. Front View

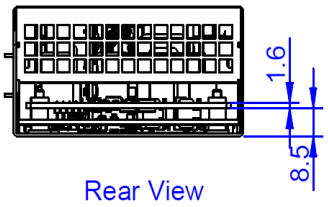


Figure 16. Rear View

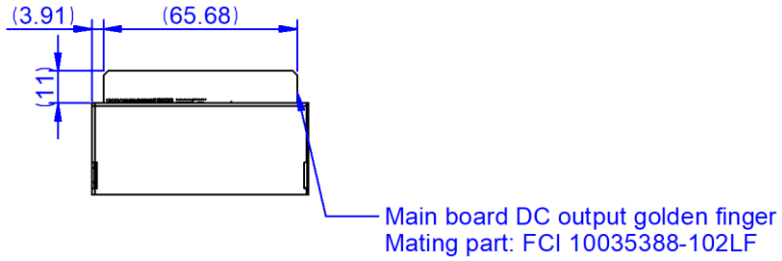


Figure 17. Mating Connector FCI 10035388-102LF

14. CONNECTIONS

The AC input receptacle shall be a 3 pins IEC320 C14 inlet. This inlet shall be rated for operation at 15A/250 VAC.
For the pin assignment of DC connector, please refer to Figure 18 and Table 4.

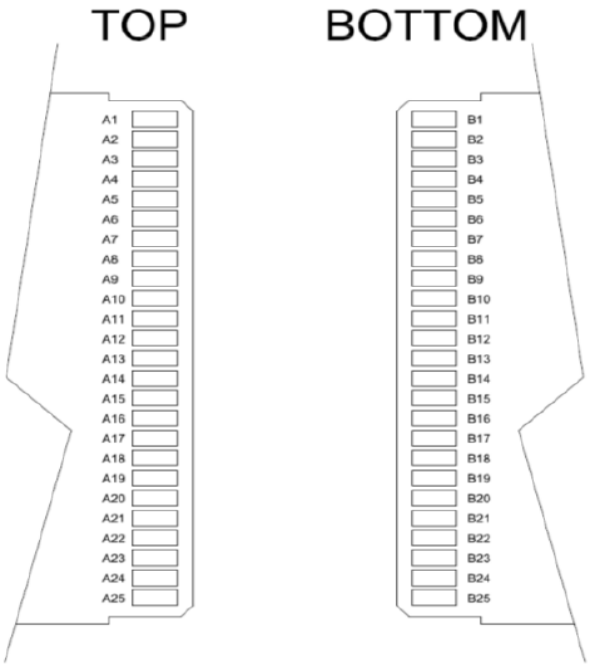
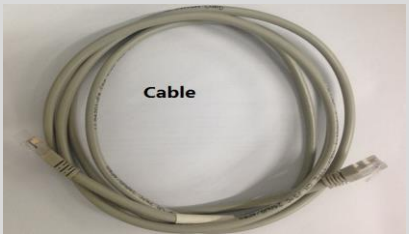


Figure 18. Pin Assignment of DC Connector

PIN	SIGNAL NAME	DESCRIPTION
A1 ~ A9	VS_R	+12 V return
B1 ~ B9	VS_R	+12 V return
A10 ~ A18	VS	+12 V power output
B10 ~ B18	VS	+12V power output
A19	SDA	I²C Data signal
A20	SCL	I²C Clock signal
A21	PS_ON	Module PS_ON Remote control power On/Off (Pulled LOW=POWER ON)
A22	SMB_ALERT	SMB Alert signal output: active-low
A23	VS_SENSE_R	+12 V Remote sense return
A24	VS_SENSE	+12 V Remote sense
A25	PWOK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.
B19	A0	I²C address bit 0
B20	A1	I²C address bit 1
B21	12 VSB	+12 V Standby Output
B22	PDB_FAULT	To receive a FAULT signal from system or PSU backplane. PSU shall shutdown if this pin is pulled HIGH.
B23	ISHARE	+12 V Main output Current share bus
B24	PDB_ALERT	To receive ALERT signal from system or PSU backplane, If signal is pulled LOW, the PSU internal fan shall be forced to run at maximum speed to improve thermal performance.
B25	Present_L	Power supply seated, active-low

15. ACCESSORIES

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ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**BPS I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PET Front-Ends (and other I²C units)	Download	belfuse.com/power-solutions
  	**Dual Connector Board** Connector board to operate 2 PET units in parallel. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	VRA.00334.0	Bel Power Solutions

For more information on these products consult: tech.support@psbel.com

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TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.