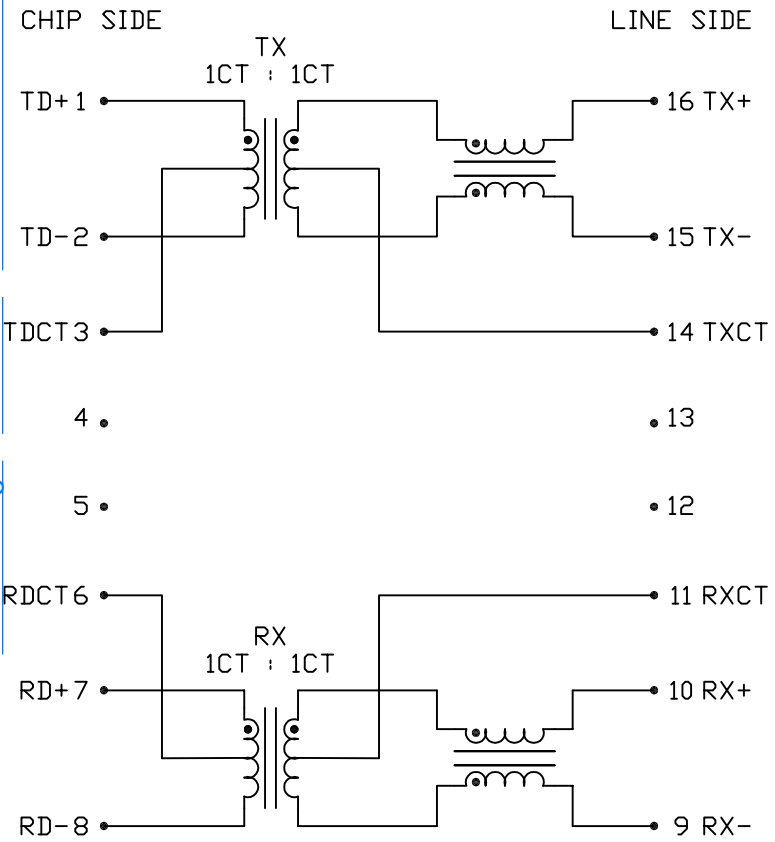


Additional Resources: Product Page 3D Model Technical Documentation

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SCHEMATIC



ELECTRICAL CHARACTERISTICS @ 25°C

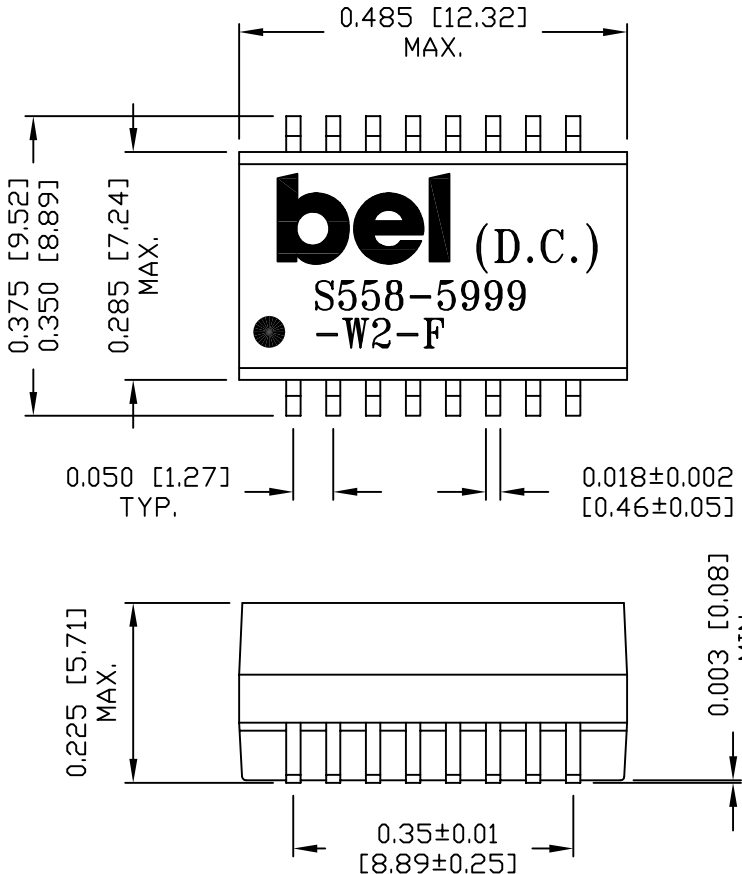
Turns Ratio	1CT : 1CT
Tx (1-3-2) : (16-14-15)	1CT : 1CT
Rx (7-6-8) : (10-11-9)	
Polarity	PER DOT CONVENTION
OCL	350μH MIN
1-2 = 7-8	@100kHz, 100mV W/8mA DC BIAS
Leakage Inductance, Le	0.4μH MAX
CHIP SIDE WITH LINE SIDE SHORT	@1MHz, 20mV
Interwinding Capacitance, Cw/w	25pF MAX
CHIP SIDE TO LINE SIDE	@1MHz, 20mV
DC Resistance	
(1-2) = (7-8)	1.3ΩHM MAX
Insertion Loss	1.0dB MAX
@100kHz TO 80MHz	
Return Loss (UNDER 100Ω ±15% ENVIRONMENT)	
@0.5 TO 30 MHz	16dB MIN
@30 TO 60 MHz	16-20LOG(f/30MHz) dB MIN
@60 TO 80 MHz	10dB MIN
Common to Common Mode Attenuation	
@0.1 TO 80 MHz	38dB MIN
@80 TO 125 MHz	30dB MIN
@125 TO 250 MHz	10dB MIN
Crosstalk	
@0.1 TO 80 MHz	38dB MIN
@80 TO 125 MHz	30dB MIN
@125 TO 250 MHz	10dB MIN
Common to Differential Mode Attenuation	
@0.1 TO 80 MHz	38dB MIN
@80 TO 125 MHz	30dB MIN
@125 TO 250 MHz	10dB MIN
HIPOT	LEAKAGE CURRENT LESS THAN 1mA AT 1500VAC
Operating Temperature -40°C TO +85°C	



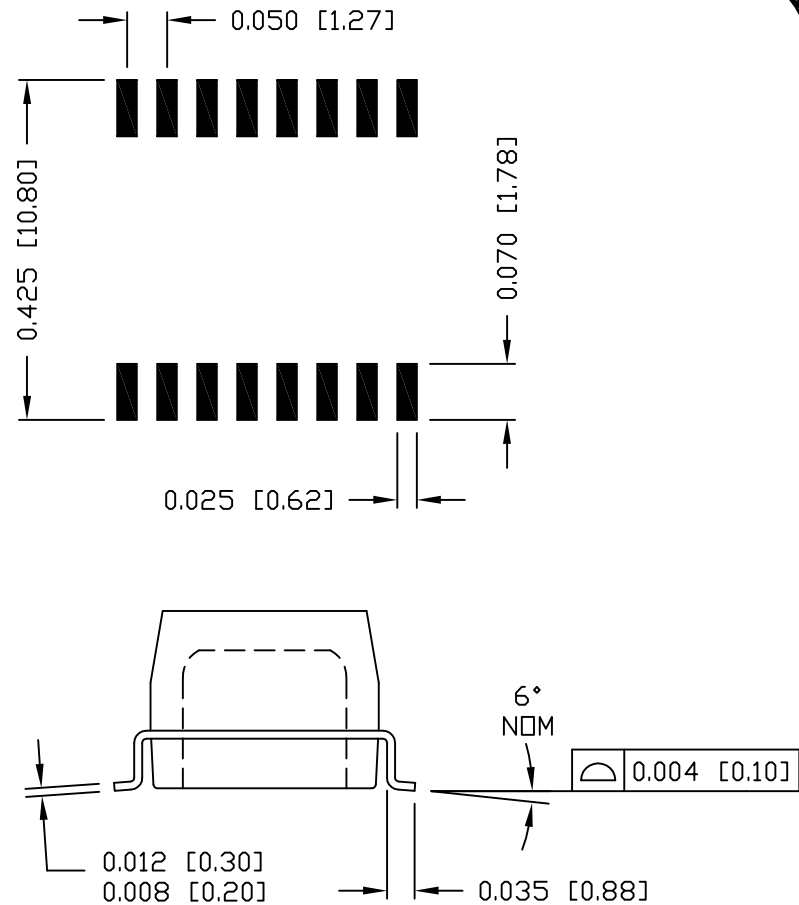
ORIGINATED BY		DATE	TITLE 10/100BASE-T MODULE S558-5999-W2-F	PART NO. / DRAWING NO.		STANDARD DIM.		[] METRIC DIM. AS REF.		 POWER PROTECT CONNECT
Alice Pang		2021-01-28		S558-5999-W2-F		TOL. IN INCH		UNIT : INCH [mm]		
DRAWN BY		DATE		FILE NAME		.X		SCALE : N/A		
ZC Guo		2021-01-28		S5585999W2FA.DWG		.XX		SIZE : A4		
						.XXX				

Additional Resources: [Product Page](#) [3D Model](#) [Technical Documentation](#)

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SUGGESTED PCB PAD LAYOUT



- NOTES:
- 1. STANDARD MARKING REFER TO DOC. HAND-WORK-04.
 - 2. PACKAGE CODE: "QBS001".

ORIGINATED BY		DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.		[] METRIC DIM. AS REF.			
Lawrence Tsang		2021-01-28			S558-5999-W2-F		TOL. IN INCH		UNIT : INCH [mm]	
DRAWN BY		DATE			FILE NAME		.X		SCALE : N/A	
ZC Guo		2021-01-28			S5585999W2FA.DWG		.XX ±0.01		SIZE : A4	
					.XXX ±0.005					



POWER | PROTECT | CONNECT