PFS1200-12-054xD

DC-DC Front End Power Supply

RoHS Compliant

The PFS1200-12-054xD is a 1200 Watt DC to DC power supply that converts DC input into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PFS1200 Series meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

KEY FEATURES

- High Efficiency, typ. 94% efficiency at half load
- Wide input voltage range: -40 to -72 VDC
- Always-On 3.3 V standby output (Option for 5 / 12 Vsb available)
- Hot-plug capable
- Parallel operation with active digital current sharing
- High density design: 45 W/in3
- Dimensions (W x H x L): 54.5 x 40 x 228.6 mm (2.15 x 1.57 x 8.98 in)
- I2C communication interface for control, programming and monitoring with Power Management Bus protocol and PSMI Protocol
- overvoltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs represent Input and Output status
- Hold up time enhancement

APPLICATIONS

- High Performance Servers
- Routers
- Switches

PFS1200-12-054xD Series
DC-DC Front-End Power Supply

1. ORDERING INFORMATION

PFS	1200	-	12	-	054	X	D
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow [1]	Input
PFS Front-Ends	1200 W		12 V		54 mm	N: Normal R: Reverse	D: DC Input

[1] N = Normal Airflow from Output connector to Input socket
R = Reverse Airflow from Input socket to Output connector

2. OVERVIEW

The PFS1200 Series DC/DC power supply is a DSP controlled, highly efficient front-end power supply. It incorporates state of the art technology and adopts boost converter and full bridge LLC which use resonance soft-switching technology, synchronous rectification to reduce component stresses, thus providing increased system reliability and very high efficiency. With a wide input DC voltage range the PFS1200 Series maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.

An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

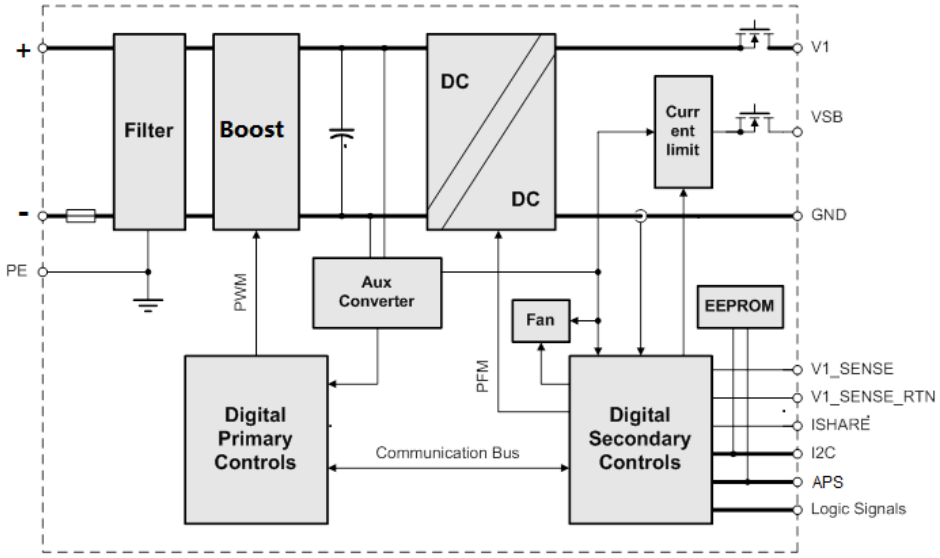


Figure 1. Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Vi *maxc*	Maximum Input Voltage	Continuous			-75	VDC

4. INPUT SPECIFICATIONS

General Condition: T_A = -20… 50°C unless otherwise specified.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	Nominal input voltage		-48		-60	VDC
V_i	Input voltage ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	-40		-72	VDC
$I_{i\,max}$	Max input current	Vi > Vi min			35	A_{rms}
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_A = 25°C, cold start			50	A_p
Vi_{VSB_on}	Turn-on standby input voltage	Ramping up	-38		-40	VDC
Vi_{VSB_off}	Turn-off standby input voltage	Ramping down	-37		-39	VDC
Vi_{V1_on}	Turn-on V1 input voltage	Ramping up	-38		-40	VDC
Vi_{V1_off}	Turn-off V1 input voltage	Ramping down	-37		-39	VDC
T_{V1_holdup}	Hold-up Time V1	V_1 > 10.8 V, V_{SB} within regulation, V_i = -48 VDC, $P_{0\,nom}$ *(from DC input lost to V1 lost to 10.8V)*	1			ms
T_{VSB_holdup}	Hold-up time Vsb	Vsb full load	5			ms

4.1 INPUT FUSE

A fast-acting 50A input fuse in the negative voltage path inside the power supply protect against severe defects. The fuse is not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

Internal bulk capacitors will be charged through resistors connected from bulk cap minus pin to the DC rail minus, thus limiting the inrush current. After the inrush phase, NTC resistors are then shorted with MOSFETs connected in parallel. The Inrush control is managed by the digital controller (DSP).

4.3 INPUT UNDER-VOLTAGE

If the input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 EFFICIENCY

The topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

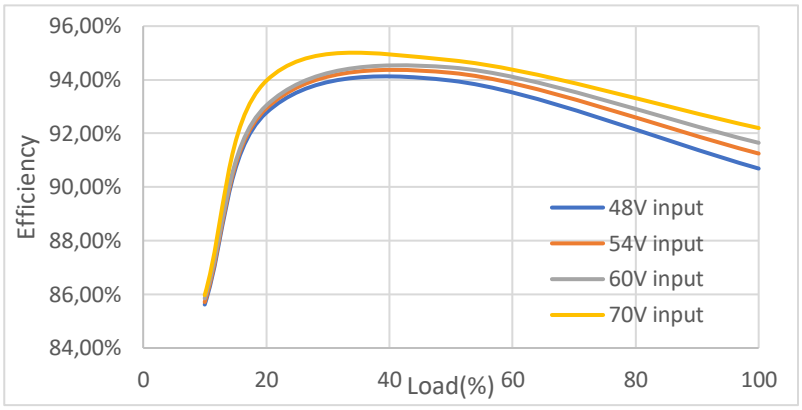


Figure 2. Efficiency Vs Load

4.5 HOLD UP TIME ENHANCEMENT

The PSU can do hold up time enhancement through adding capacitor parallel with the input connector. The PSU uses advance technology that use up the energy in the parallel cap. The table 1 shows the hold up time vs different parallel cap under different input voltage.

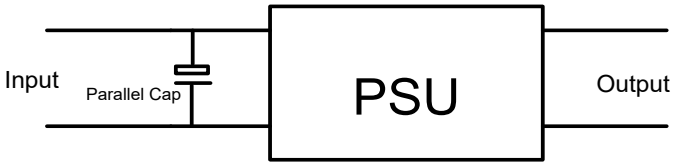


Figure 3. Parallel Cap parallel with input connector

Parallel Capacitance (uF)	Hold up time (ms)			
	40V input	48V input	60V input	72V input
0	2.8	3.0	3.3	3.6
820	3.4	3.7	4.4	5.3
1640	3.9	4.5	5.6	6.9
2460	4.4	5.2	6.7	8.6
3280	4.8	5.9	7.8	10.1
4100	5.4	6.5	8.9	11.8

Table 1. Hold Up Time Vs. Different Parallel Capacitance

4.6 DC LINE TRANSIENT TEST

MINUS 72 VDC LINE TRANSIENT TEST

A standard line voltage momentary transient test is shown below. This test simulates a momentary voltage overshoot. This should not affect the operation of the PSU, the output voltage should remain in regulation. This test shall be conducted every 10 sec for 30 min (180 times total).

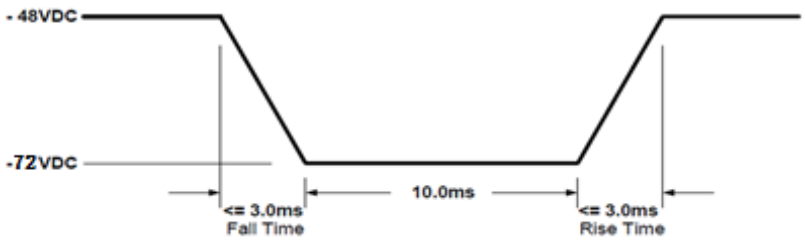


Figure 4. Minus 72 VDC Line Transient Test

0 V LINE TRANSIENT TEST

A standard line voltage momentary blackout test is shown below. This test simulates a momentary switch throw off-on, see graph below. The power supply should restart, not latch. This test shall be conducted 3 times in 10 min intervals.
Practically a blackout of any duration should not damage the power supply in any way and not cause a latch off condition.

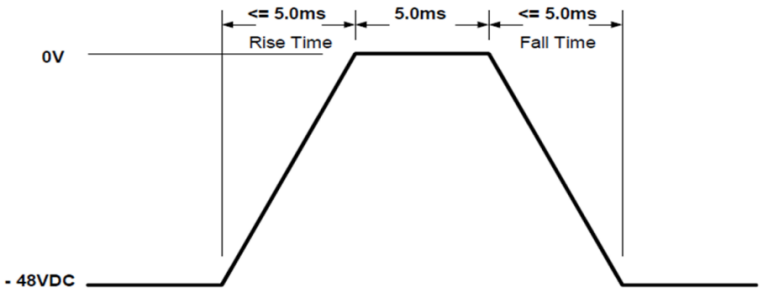


Figure 5. 0 V Line Transient Test

5. OUTPUT SPECIFICATIONS

General Condition: T_A = -20… 50°C unless otherwise specified.

PARAMETER		CONDITIONS / DESCRIPTION		MIN	NOM	MAX	UNIT
Main Output V_1							
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_{amb} = 25 °C			12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy			-0.5		+0.5	% $V_{1\ nom}$
d $V_{1\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-2		+2	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	V_1 = 12 VDC			1200		W
$I_{1\ nom}$	Nominal Output Current	V_1 = 12 VDC			100		A
$V_{1\ pp}$	Output Ripple Voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW, (See Section 5.1)				120	mVpp
d $V_{1\ Load}$	Load Regulation	V_1 = $V_{1\ nom}$, 0 - 100 % $I_{1\ nom}$			80		mV
d $V_{1\ Line}$	Line Regulation	V_1 = $V_{1\ min}$... $V_{1\ max}$			40		mV
d I_{share}	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 20%		-5		+5	%
d V_{dyn}	Dynamic Load Regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 0.5 A/µs, 2000 µF low ESR capacitive loading		-0.6		0.6	V
T_{rec}	Recovery Time	recovery within 1% of $V_{1\ nom}$			2		ms
$T_{DC\ V1}$	Start-Up Time From DC	V_1 = 10.8 VDC				2	sec
$t_{V1\ rise}$	Rise Time	V_1 = 10…90% $V_{1\ nom}$		1		20	ms
tV1 ovr sh	Output Turn-on Overshoot	*Vi nom*, 0 to 100% *I1 nom*				0.6	V
dV1 sense	Remote Sense	Compensation for cable drop, 0 to 100% *I1 nom*				0.25	V
C_{Load}	Capacitive Loading	T_a = 25 °C		1000		20 000	µF
3.3 / 5 V_{SB} Standby Output							
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL1 = 1 VSB_SEL2 = 1		3.3		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		VSB_SEL1 = 0 VSB_SEL2 = 1		5.0		VDC
			1	-1		+1	% V_{1nom}
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-3		+3	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	V_{SB} = 3.3 VDC			16.5		W
		V_{SB} = 5.0 VDC			16.5		
$I_{SB\ nom}$	Nominal Output Current	V_{SB} = 3.3 VDC			5		A
		V_{SB} = 5.0 VDC			3.3		
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW, (See Section 5.1)				100	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\ nom}$	VSB_SEL1 = 0 VSB_SEL2 = 1		67		mV
			VSB_SEL1 = 1 VSB_SEL2 = 1		44		
$I_{SB\ max}$	Current Limitation	VSB_SEL1 = 0, VSB_SEL2 = 1		5.25		6	A
		VSB_SEL1 = 1, VSB_SEL2 = 1		3.45		4.3	
dV_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_0/dt = 0.5A/µs, recovery within 1% of $V_{1\ nom}$		-3		3	% V_{SBnom}
T_{rec}	Recovery Time					250	µs
$T_{DC\ VSB}$	Start-up Time from DC	V_{SB} = 90% $V_{SB\ nom}$				2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$		0.5		30	ms
C_{Load}	Capacitive Loading	T_{amb} = 25°C		100		1500	µF

12 V_{SB} Standby Output							
$V_{SB\ nom}$	Nominal Output Voltage	0.5 · $I_{SB\ nom}$, T_{amb} = 25°C	VSB_SEL1 = 1		12		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		VSB_SEL2 = 0	-1		+1	% $V_{1\ nom}$
$dV_{SB\ tot}$	Total Regulation	$V_{1\ min}$ to $V_{1\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$		-3		+3	% V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power				24		W
$I_{SB\ nom}$	Nominal Output Current				2		A
$V_{SB\ pp}$	Output Ripple Voltage	$V_{SB\ nom}$, $I_{SB\ nom}$, 20 MHz BW, (See Section 5.1)			60	120	mVpp
d V_{SB}	Droop	0 - 100 % $I_{SB\ nom}$			250		mV
d V_{SBdyn}	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 5 … 100% $I_{SB\ nom}$, dI_o/dt = 0.5 A/µs, recovery within 1% of $V_{1\ nom}$		-5		+5	% V_{SBnom}
T_{rec}	Recovery Time				2		ms
$T_{DC\ VSB}$	Start-Up Time from DC Input	V_{SB} = 90% $V_{SB\ nom}$				2	sec
$t_{VSB\ rise}$	Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$		4		20	ms
C_{Load}	Capacitive Loading	T_{amb} = 25 °C		100		1500	µF

5.1 RIPPLE / NOISE

Internal capacitance at the 12 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors (a parallel combination of 10 µF tantalum capacitor in parallel with 0.1 µF ceramic capacitors) should be added close to the power supply output.
The setup of *Figure 6.* has been used to evaluate suitable capacitor types. The capacitor combinations of *Table 2* and *Table 3* should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

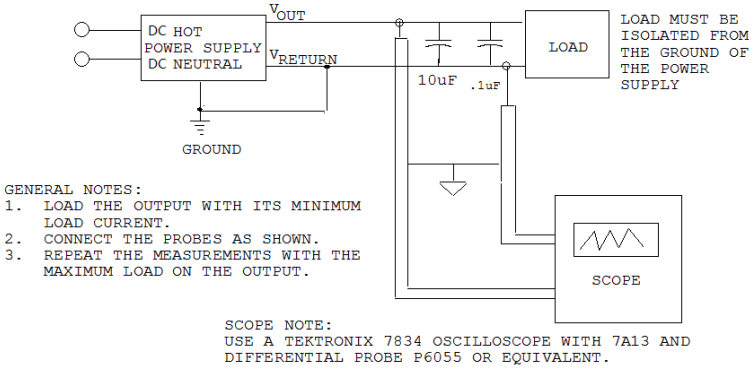


*Figure **6**. Output ripple test setup*

NOTE: Care must be taken when using ceramic capacitors with a total capacitance of 1 µF to 50 µF on output V1, due to their high-quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

EXTERNAL CAPACITOR V1	DV1MAX	UNIT
Standard test condition: 1 Pcs 10 µF / 63 V Electrolytic Capacitor 1 Pcs 0.1 µF / 100 V ceramic capacitor	150	mVpp
1Pcs 1000µF/16V/Low ESR Aluminum/ø10x20	120	mVpp

Table 2. Suitable capacitors for V_1

EXTERNAL CAPACITOR VSB	DV1MAX	UNIT
Standard test condition: 1 Pcs 10 µF / 63 V Electrolytic Capacitor 1 Pcs 0.1 µF / 100 V ceramic capacitor	120	mVpp
1 Pcs 100µF/16V/Low ESR Aluminum/ø5x10	100	mVpp

Table 3. Suitable capacitors for VSB

The output ripple voltage on V_{SB} is influenced by the main output V_1. Evaluating V_{SB} output ripple must be done when maximum load is applied to V_1.

6. PROTECTION SPECIFICATIONS

General Condition: T_A = -20… 50°C unless otherwise specified.

PARAMETER		DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
F	Input Fuse	Not user accessible			50		A
$V_{1\ OV}$	OV Threshold V_1			13.0		14.5	VDC
$t_{OV\ V1}$	OV Latch Off Time V_1	V1 with half load			1		ms
$V_{SB\ OV}$	OV Threshold V_{SB}			110		120	% V_{SB}
$t_{OV\ VSB}$	OV Latch Off Time V_{SB}	Vsb with half load			1		ms
$I_{V1\ lim}$	Over Current Limitation V_1	T_a < 50°C		105		130	A
$I_{VSB\ lim}$	Over Current Limitation V_{SB}	T_a < 50°C for	12 V_{SB}	2.2		2.8	A
			5.0 V_{SB}	3.45		4.5	
			3.3 V_{SB}	5.25		6.2	
$t_{V1\ SC}$	Short Circuit Regulation Time	V_1 < 3 V, time until I_{V1} is limited to < $I_{V1\ sc}$				2	ms
T_{SD}	Over Temperature on Heat Sinks	Automatic shut-down			115		°C

6.1 OVERVOLTAGE PROTECTION

The PFS front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the DC mains or by toggling the PSON_L input.

6.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored.

12 V_{SB}
LED and PWOK_L pin signal if the output voltage exceeds ±7% of its nominal voltage. Output under voltage protection is provided on both outputs. When either V1 or VSB falls below 93% of its nominal voltage, the output is inhibited.

3.3 / 5 V_{SB}
LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage. Output under voltage protection is provided on the standby output only. When VSB falls below 75% of its nominal voltage, the main output V1 is inhibited.

6.3 CURRENT LIMITATION

6.3.1 MAIN OUTPUT

When main output runs in current limitation mode its output will turn OFF below 2 V but will retry to recover every 1 s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retries from current limitation mode.

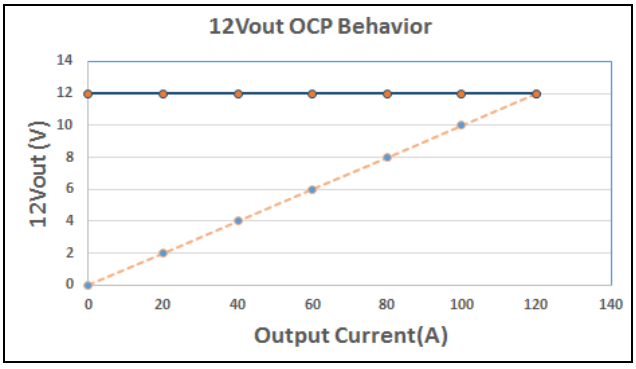


Figure 7. Current Limitation on V1

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 50°C.

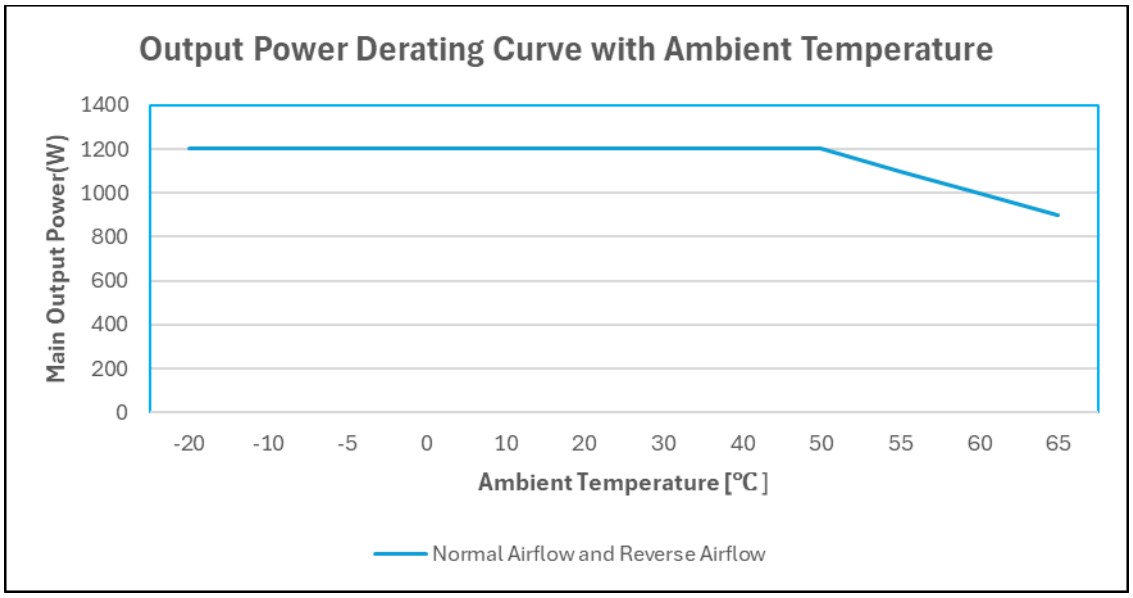


Figure 8. Derating Curve for ambient above 50°C

6.3.2 STANDBY OUTPUT

3.3 / 5 V_{SB}

The standby output exhibits a substantially rectangular output characteristic down to 0 V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the DC input voltage.

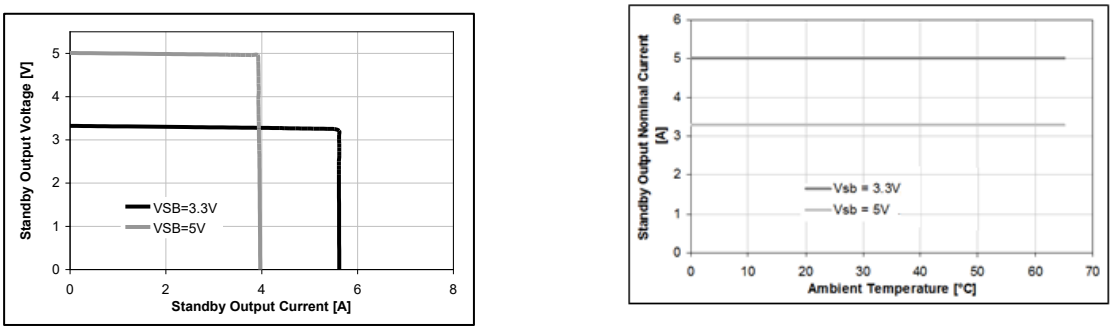


Figure 9. Current Limitation and Temperature Derating on 3.3 / 5 V_{SB}

12 V_{SB}

On the standby output, a hiccup type over current protection is implemented. This protection will shut down the standby output immediately when standby current reaches or exceeds $I_{VSB\ lim}$. After an off-time of 1s the output automatically tries to restart. If the overload condition is removed the output voltage will reach again its nominal value. At continuous overload condition the output will repeatedly trying to restart with 1s intervals. A failure on the Standby output will shut down both Main and Standby outputs.

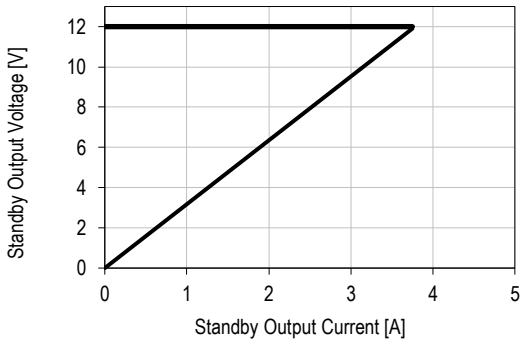


Figure 10. Current Limitation on 12 V_{SB}

7. MONITORING

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
$V_{I\,mon}$	Input Voltage	$V_{I\,min} \le V_I \le V_{I\,max}$	-2		+2	VDC
$I_{I\,mon}$	Input Current		-1		+1	A
$P_{I\,mon}$	True Input Power	I1 > 25 A I1 ≤ 25 A	-5 25		+5 25	% W
$V_{1\,mon}$	V_1 Voltage		-2		+2	%
$I_{1\,mon}$	V_1 Current	I1 > 25 A, T_{amb} = 25°C I1 ≤ 25 A, T_{amb} = 25°C	-2 -1.5		+2 +1.5	% A
$P_{o\,nom}$	Total Output Power	Po > 120 W Po ≤ 120 W	-5 -15		+5 +15	% W
$V_{SB\,mon}$	Standby Voltage		-0.3		+0.3	V
$I_{SB\,mon}$	Standby Current	$I_{SB} \le I_{SB\,nom}$	-0.5		+0.5	A

8. SIGNAL & CONTROL SPECIFICATIONS

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs						
V_{IL}	Input Low Level Voltage		-0.2		0.8	V
V_{IH}	Input High Level Voltage		2.4		3.5	V
$I_{IL, H}$	Maximum Input Sink or Source Current		0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H			100		kΩ
R_{puPSON_L}	Internal Pull Up Resistor on PSON_L			10		kΩ
$R_{puHOTSTANDBYEN\_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H			10		kΩ
R_{LOW}	Resistance Pin to SGND for Low Level		0		1	kΩ
R_{HIGH}	Resistance Pin to SGND for High Level		50			kΩ
PWOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 4 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 0.5 mA	2.6		3.5	V
R_{puPWOK_H}	Internal Pull Up Resistor on PWOK_H			1		kΩ
VINOK_H Output						
V_{OL}	Output Low Level Voltage	I_{sink} < 2 mA	0		0.4	V
V_{OH}	Output High Level Voltage	I_{source} < 50 µA	2.6		3.5	V
$R_{puVINOK\_H}$	Internal Pull Up Resistor on VINOK_H			10		kΩ
SMB_ALERT_L Output						
V_{ext}	Maximum External Pull Up Voltage				12	V
V_{OL}	Output Low Level Voltage	I_{source} < 4 mA	0		0.4	V
I_{OH}	Maximum High Level Leakage Current				10	µA
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L			None		kΩ

8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off. If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal Schottky diodes, except for SMB_ALERT_L, ISHARE and I²C pins. SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V Zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

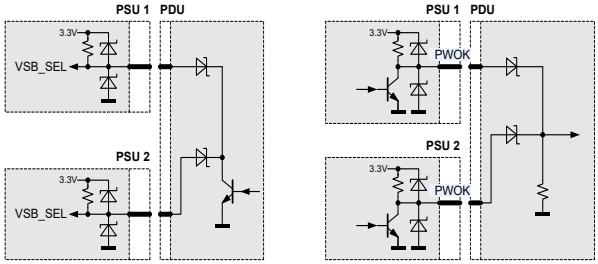


Figure 11. Interconnection of Signal Pins

8.3 FRONT LEDS

There are two Bi-color (Green/ Amber) LEDs to indicate power supply status. The LEDs are visible on the power supply's front panel. The LEDs location meets ESD Requirements. Following are these definitions as:

LED FUNCTION	COLOR	BRIGHTNESS
Input Status LED	Green (520 nm – 540 nm) / (Amber color not used)	500-1000cd/m^2
Output Status LED	Green (520 nm – 540 nm) / Amber (520 nm – 540 nm) Amber (587 nm – 595 nm)	500-1000cd/m^2

OPERATING CONDITION	LED BEHAVIOR	
CONDITION	INPUT STATUS LED	OUTPUT STATUS LED
Output ON and OK	GREEN Solid	GREEN Solid
No Input power to all power supplies	OFF	OFF
Power supply warning events where the power supply continues to operate: high temp, high power, high current, over voltage, under voltage, slow fan.	GREEN Solid	1Hz AMBER/GREEN Blinking
Power supply critical event causing a shutdown: failure, OCP, SCP, OVP, UVP, OTP, Fan Fail	GREEN Solid	AMBER Solid
Input over voltage shutdown	1Hz GREEN Blinking	AMBER Solid
Input under voltage shutdown	1Hz GREEN Blinking	OFF
PS_KILL	GREEN Solid	OFF
Input present / Only 12VSB on (PS off)	GREEN Solid	1Hz Blinking GREEN
Power supply in FW upload mode	GREEN Solid	2Hz Blinking GREEN

AMBER/GREEN BLINKING: means AMBER and GREEN LED flash alternately.

Table 4. LED Status

8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

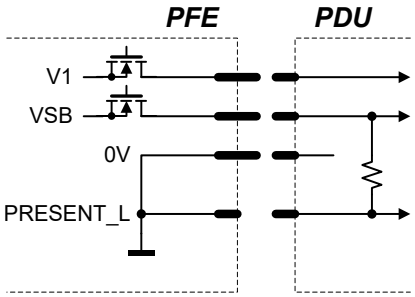


Figure 12. PRESENT_L signal pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 VINOK_H

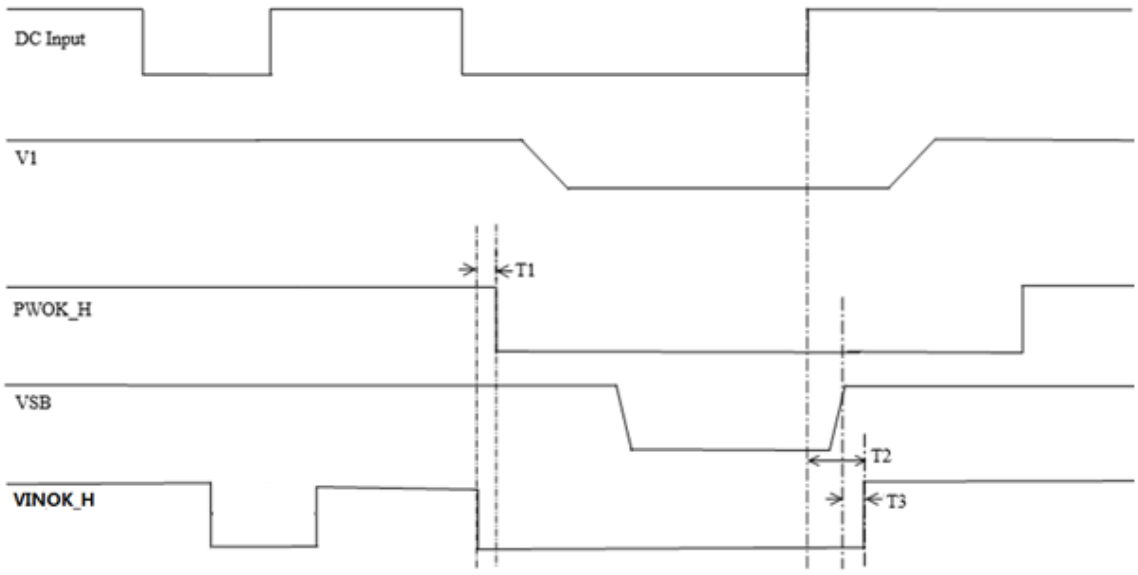


Figure 13. VINOK_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H & PWOK_H	0.5			ms
T2	VIN_OK_H delay to DC			1700	ms
T3	VIN_OK_H to VSB			20	ms

Table 5. VINOK_H Timing Requirement

8.7 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (Tvout_rise) within 1 to 70 ms. All outputs must rise monotonically. The Table below shows the timing requirements for the power supply being turned on and off two ways; 1) via the DC input with PSON_L held low; 2) via the PSON_L signal with the DC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

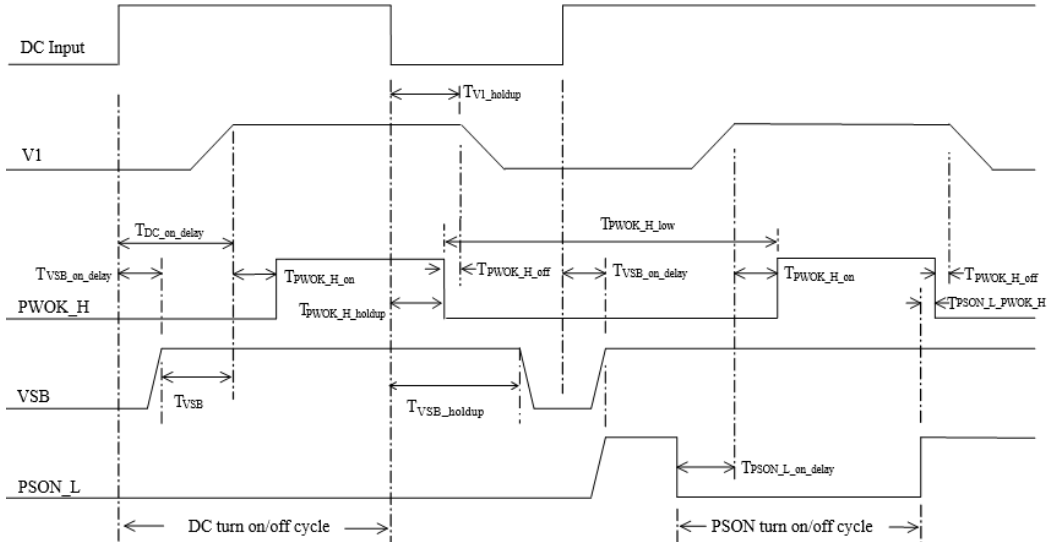


Figure 14. Timing Requirement

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_{V1_rise}	Output voltage rise time	1.0		70	ms
$T_{VSB\_on\_delay}$	Delay from DC being applied to VSB being within regulation.			1500	ms
$T_{DC\_on\_delay}$	Delay from DC being applied to all output voltages being within regulation.			3000	ms
T_{V1_holdup}	Time 12 V output voltage stay within regulation after loss of DC.	2			ms
$T_{PWOK\_H\_holdup}$	Delay from loss of DC to de-assertion of PWOK_H	1			ms
$T_{PSON\_L\_on\_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON\_L\_PWOK\_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
$T_{PWOK\_H\_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK\_H\_off}$	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	0.5			ms
$T_{PWOK\_H\_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using PSON_L signal.	100			ms
T_{VSB}	Delay from VSB being in regulation to O/Ps being in regulation at DC turn on.	50		1000	ms
T_{VSB_holdup}	Time the VSB output voltage stays within regulation after loss of DC.	5			ms
$T_{DC\_off\_SMB\_ALERT\_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of DC input voltage.			2	ms

8.8 CURRENT SHARE

The PFS front-ends have an active current share scheme implemented for V_1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The standby output uses a passive current share method (droop output voltage characteristic).

8.9 VSB VOLTAGE SELECTION (VSB_SEL1, VSB_SEL2)

The standby output voltage can be configured to three different values: 3.3V, 5V and 12V by pulling VSB_SEL1 and VSB_SEL2 input pins either to GND (Logic Low) or to 3.3V

VSB_SEL1	VSB_SEL2	VSB Voltage	UNIT
1	1	3.3	V
0	1	5	V
1	0	12	V
0	0	Invalid (Off)	

8.10 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its Oring gate. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN_H pin is high, the load current is low and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I^2C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

Asia-Pacific
+86 755 2988 5888

EMEA
+353 61 531 820

North America
+1 408 513 2839

powersupport@belf.com
belfuse.com

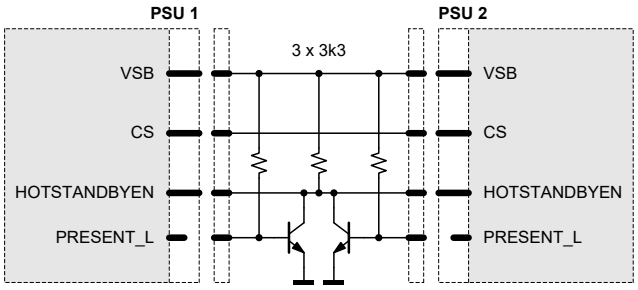


Figure 15. Recommended hot-standby configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure 15.* If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

8.12 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

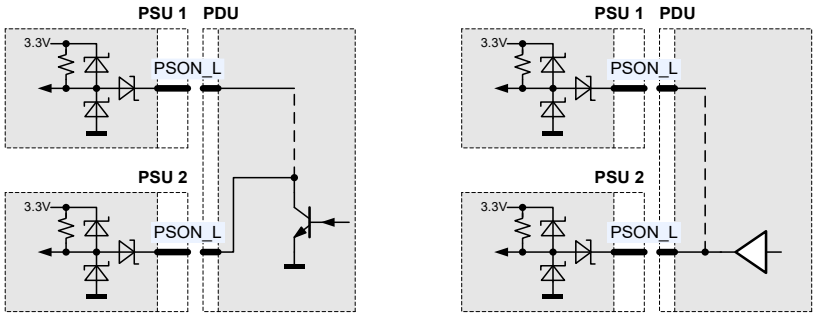


Figure 16. PSON_L connection

8.13 I2C / SMBUS COMMUNICATION

The interface driver in the PFS supply is referenced to the V1 Return. The PFS supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in *Table 6* further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

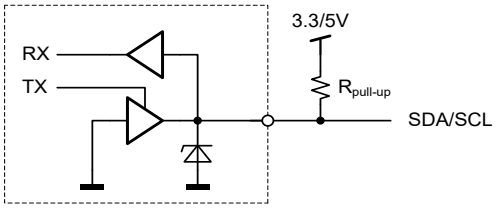


Figure 17. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB_ALERT_L call address 25(0x19) by sending its status register.

Communication to the DSP or the EEPROM will be possible as long as the input DC voltage is provided. If no DC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

PARAMETER	DESCRIPTION / CONDITION		MIN	NOM	MAX	UNIT
V_{iL}	Input low voltage		-0.5		1.0	V
V_{iH}	Input high voltage		2.3		5.5	V
V_{hys}	Input hysteresis		0.15			V
V_{oL}	Output low voltage	3 mA sink current	0		0.4	V
t_r	Rise time for SDA and SCL		20+0.1Cb1		300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < Cb^2 < 400 pF	20+0.1Cb^2		250	Ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10		10	µA
C_i	Internal Capacitance for each SCL/SDA				50	pF
f_{SCL}	SCL clock frequency		0		100	kHz
R_{pu}	External pull-up resistor	f_{SCL} ≤ 100 kHz			1000 ns / Cb	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0			µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0			µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7			µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0		3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250			ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0			µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5			ms

Table 6. I2C / SMBus Specification

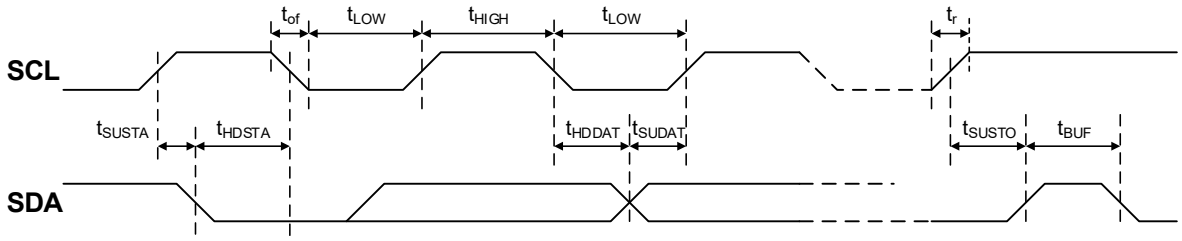


Figure 18. I2C / SMBus Timing

1 Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

8.14 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTES:

- If the APS pin is left open, the supply will operate with the Power Management Bus protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change address dynamically.

R_{APS} (Ω) [2]	Protocol	I2C Address [3]	
		Controller	EEPROM
820	Power Management Bus	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6

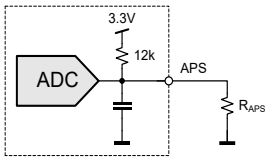


Figure 19. I2C address and protocol setting

8.15 CONTROLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure 20*). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default, the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

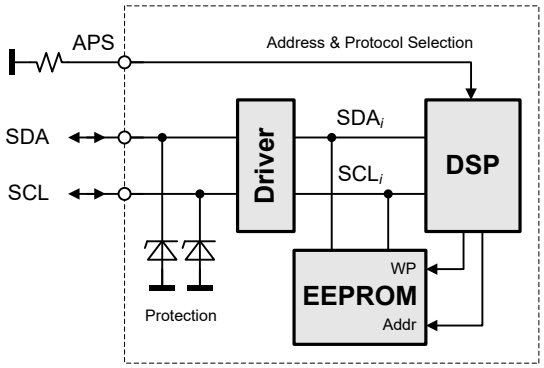


Figure 20. I2C Bus to DPS and EEPROM

1 E12 resistor values, use max 5% resistors
2 The LSB of the address byte is the R/W bit

8.16 EEPROM PROTOCOL

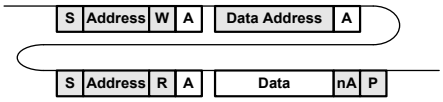
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



8.17 POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

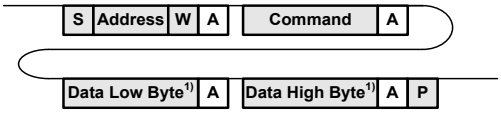
Power Management Bus command codes are not register addresses. They describe a specific command to be executed.

The PFS1200 supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

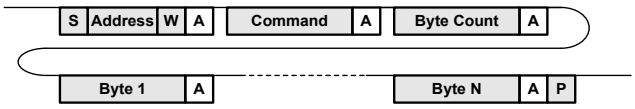
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



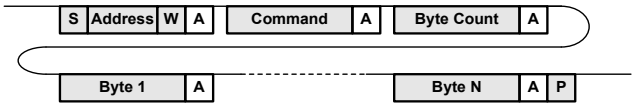
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFS Programming Manual for further information.

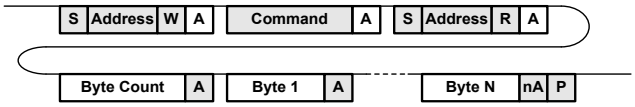


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFS Programming Manual BCA.00006 for further information.



8.18 GRAPHICAL USER INTERFACE

Bel Power Solutions provide with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFS1200 Front-End. The utility can be downloaded on: belfuse.com and supports Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G2Q01.0 Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

NOTE: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

9. TEMPERATURE AND FAN CONTROL

To achieve the best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFS1200-12-054ND PSU is provided with normal airflow, which means the air enters through the DC output connector side of the supply and leaves at the DC input connector side. PFS supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the DC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the DC-inlet.

NOTE: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

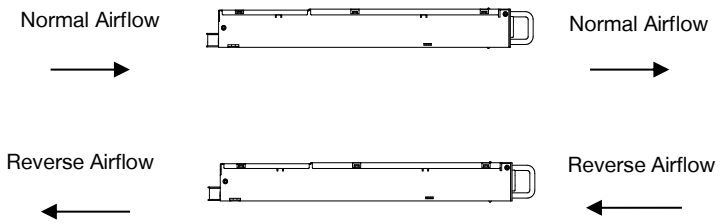


Figure 21. Airflow direction

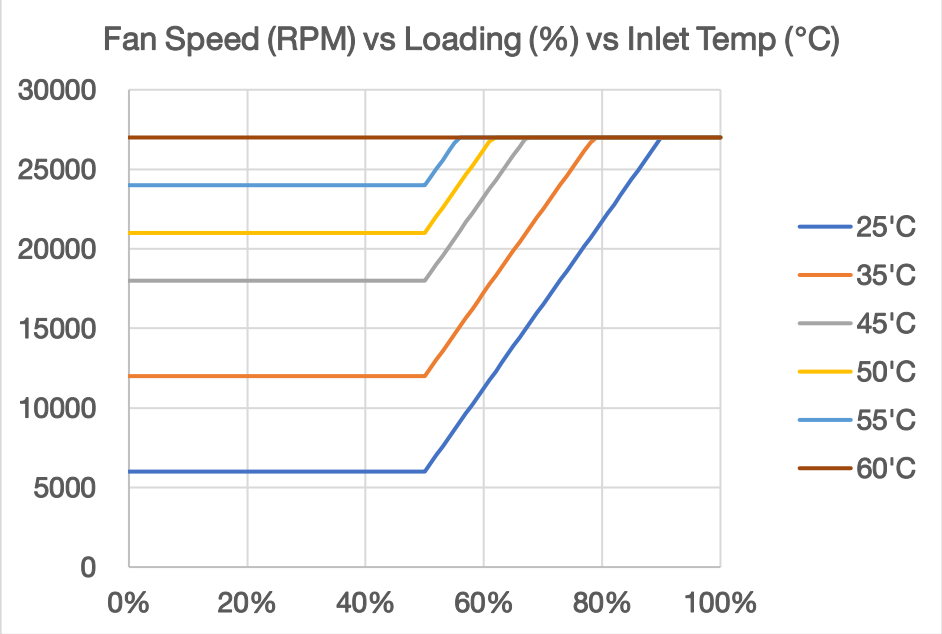


Figure 22. Fan speed vs. main output load

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55035.

TEST	STANDARD / DESCRIPTION	CRITERIA
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	EN 55024: 2010/A1: 2015 using the IEC 61000-4-3: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24	A
Burst	IEC / EN 61000-4-4, level 3 Input DC port ±1 kV, 1 minute DC port ±0.5 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: ±1 kV Line to line: ±0.5 kV	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW.	A

10.2 EMISSION

TEST	STANDARD / DESCRIPTION	CRITERIA
Conducted Emission	EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, single unit. EN55032 / CISPR 32: 0.15 … 30 MHz, QP and AVG, 2 units in rack system.	Class A Class A
Radiated Emission	EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, single unit. EN55032 / CISPR 32: 30 MHz … 1 GHz, QP, 2 units in rack system.	Class A Class A

11. SAFETY APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL/ CSA 62368-1 (USA / Canada) EN62368-1 (Europe) IEC62368-1 (International) CB Certificate & Report,IEC 62368-1 (report to include all country national deviations) CE - Low Voltage Directive 2014/35/EC	Approved
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Basic
	Output to chassis	None (Direct connection)
Electrical Strength Test	Input to output	1500 VDC
	Input to chassis	1500 VDC

12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{o\,nom}$, $I_{SB\,nom}$	-20		+50	°C
T_{Aext}	Extended Temp. Range	Derated output	+51		+65	°C
T_S	Storage Temperature	Non-operational	-40		+70	°C
	Altitude	Operational, above Sea Level, refer derating to Ta	-		3000	m

13. MECHANICAL SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		54.5		mm
	Height		40.0		
	Depth		228.6		

PFS1200-12-054xD Series

DC-DC Front-End Power Supply

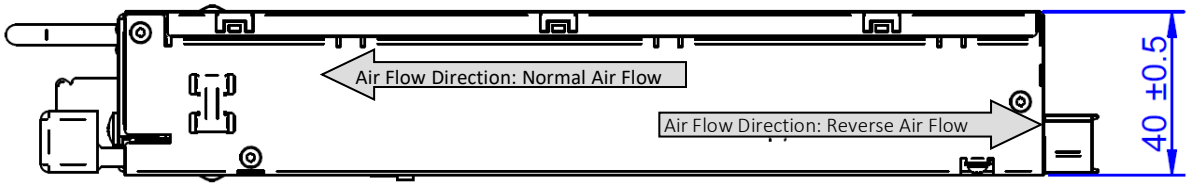


Figure 23. Side View 1

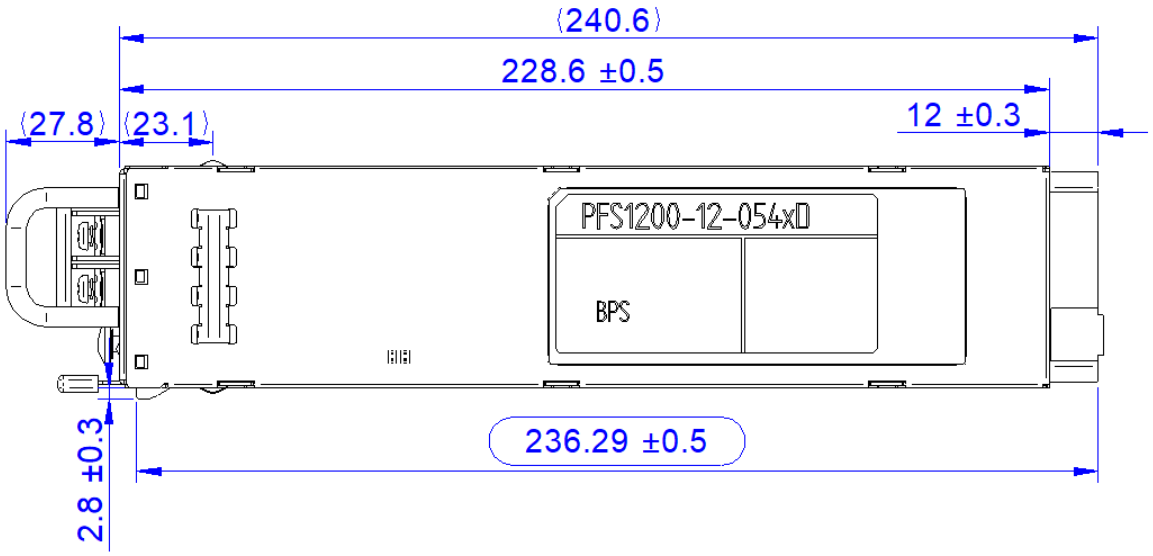


Figure 24. Top View

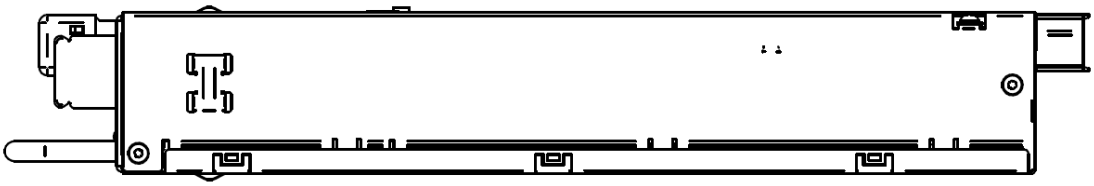


Figure 25. Side View 2

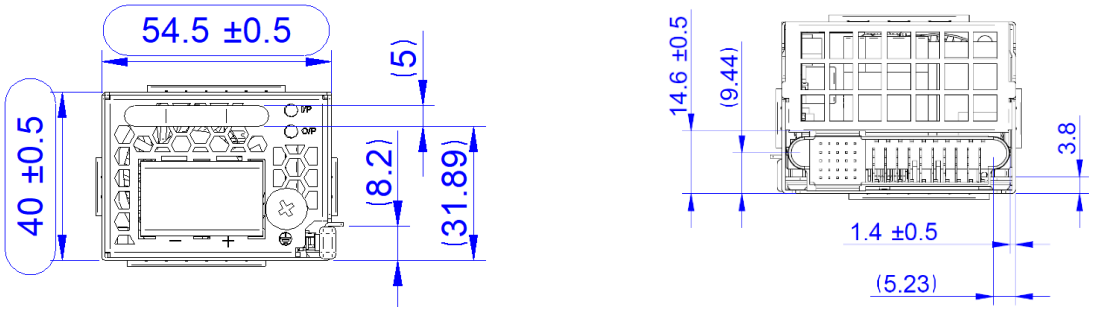
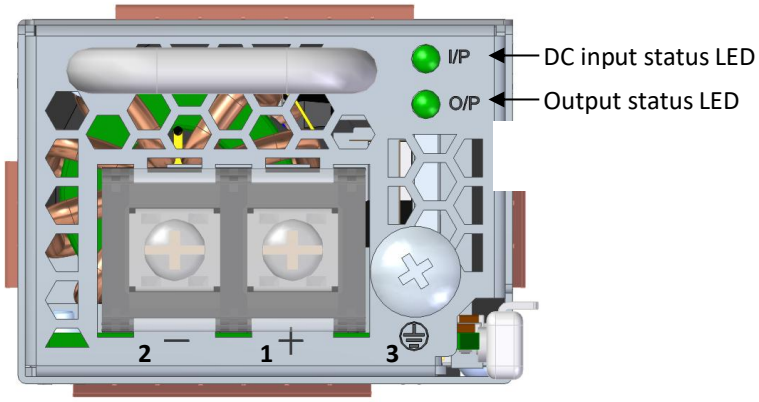


Figure 26. Front and Rear View

NOTES: A 3D step file of the power supply casing is available on request.
Unlatching the supply is performed by pulling the green trigger in the handle

14. CONNECTIONS

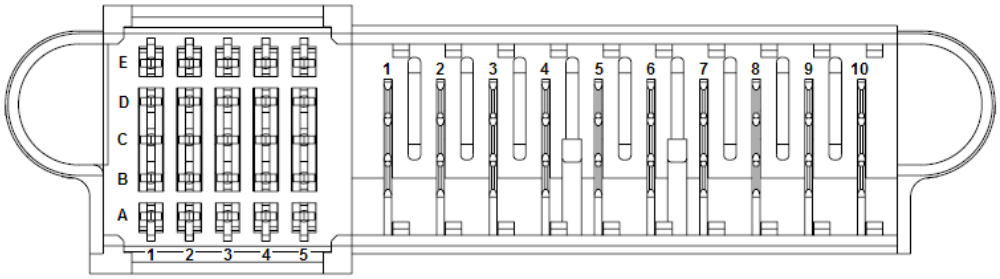
14.1 INPUT CONNECTOR (PFS1200-12-054xD)



PIN	NAME	DESCRIPTION
Input		
1	Vin+	Input positive
2	Vin-	Input negative
3	PE	Ground ⏚

DC input connector: Dinkle DT-7C-B14W-02 or equivalent

14.2 OUTPUT CONNECTOR



Power Supply Connector: Tyco Electronics P/N 1926736-3 or FCI 101-10133129-002LF or equivalent
(NOTE: Column 5 is recessed (short pins))

Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

14.2.1 PIN DEFINITION

PIN	NAME	DESCRIPTION
Output		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
Control Pins		
A1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
B1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
C1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
D1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
E1	VSB	Standby positive output (+3.3/5 V_{SB} or 12 V_{SB})
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I²C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I²C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I²C clock signal line
B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	VSB_SEL1	VSB voltage selection (See section 8.9)
E4	VINOK_H	DC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL2	Standby voltage selection (See section 8.9)
E5	PRESENT_L	Power supply present (lagging pin): active-low

Table 7. Pin Description

15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PFS Front-Ends (and other I²C units)	N/A	belfuse.com
	**Dual Connector Board** Connector board to operate 2 PFS units in parallel. Includes an on-board USB to I²C converter (use *Bel Power Solutions I²C Utility* as desktop software).	YTM.G2Q01.0	belfuse.com

16. REVISION HISTORY

DATE	REVISION	CHANGE	PREPARED BY	APPROVED BY	ECO No.
2019/01/11	1	First release	Mike Chen	-	
2019/01/11	2	Update *Block Diagram* Update efficiency curve Add hold up time enhancement	Zhiqun Wan		
2019/07/28	3	Add definition of Vsb selection	Zhiqun Wan		
2020/12/21	4	Update Max input current Update output power derating Update Input power accuracy	Rong Liang		
2020/12/21	4	Update mechanical drawing	Xiao Xue		
2021/03/15	A	Release to A	Rong Liang	Gang Wang	
2021/07/08	B	Change power supply connector from 2-1926736-3 to 1926736-3	Xiao Xue	Gang Wang	
2021/08/25	B	Add UVP and OVP LED STATUS	Rong Liang	Gang Wang	
2021/09/16	B	Change VSB VOLTAGE SELECTION Logic	Rong Liang	Gang Wang	
2023/04/14	C	Update the fuse NOM value from 40A to 50A Update output current accuracy condition T_{amb} = 25°C Update front LEDs status Update the front panel figure Change format of some text	XiaoGang Luo	Gang Wang	
2023/07/20	D	Simplify the LED status condition description in Table 4.	XiaoGang Luo	Gang Wang	CO129050
2023/08/18	E	Update the safety approve standard at section 11 Delete the tolerance spec at section 13 Add or equivalent for section 14.1 input connector Update the PSU output connector MPN and add or equivalent at section 14.2	Xiao Xue	Andrew Li	CO129539
2025/09/17	F	Update the operating temperature from 0°C to -20°C. (The change is implemented on the PFS1200-12-054RD with ID BEL REVISION 004 and later, and PFS1200-12-054ND with ID BEL REVISION 009 and later)	XiaoGang Luo	Gang Wang	C0143688

For more information on these products consult: powersupport@belf.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

