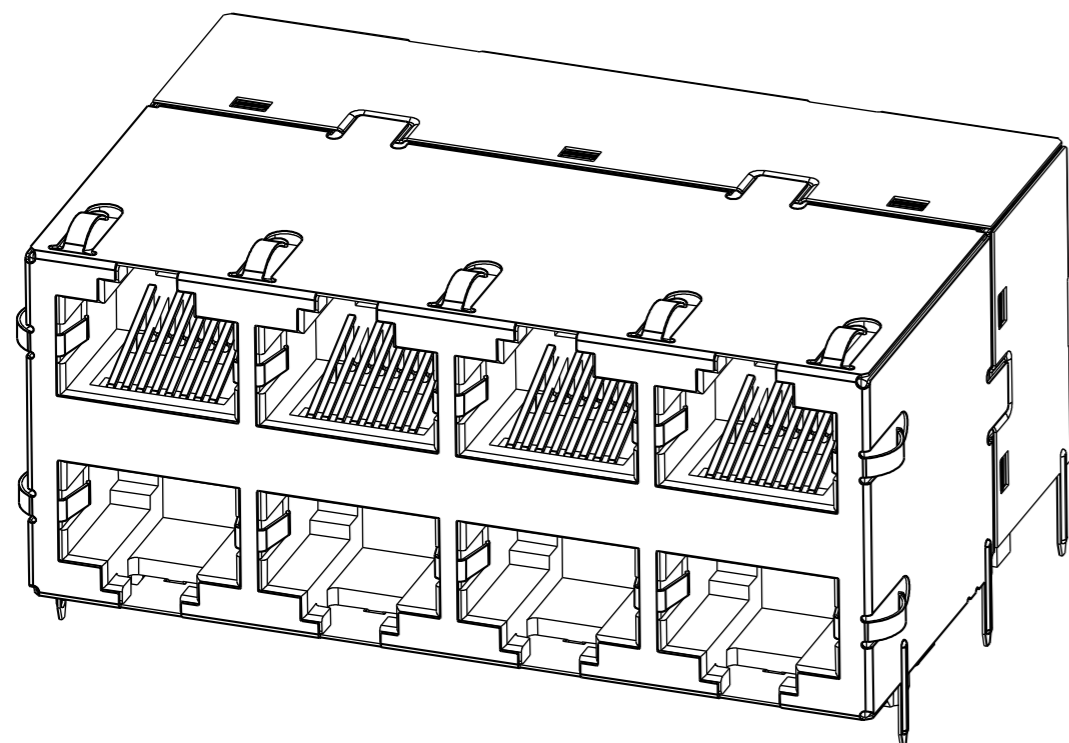


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PRODUCT MAY BE PROTECTED BY ONE OR MORE OF THE FOLLOWING US PATENTS:
 5736910 5939955 6425781 6428361 6554638 6840817 7123117
 7429195 7717749 7808751 6217391 6149050 7924130

REVISIONS				
REV	DATE	DESCRIPTION	APPD	CHKD
2	07JAN2015	COMPANY LOGO CHANGE	RL	TY

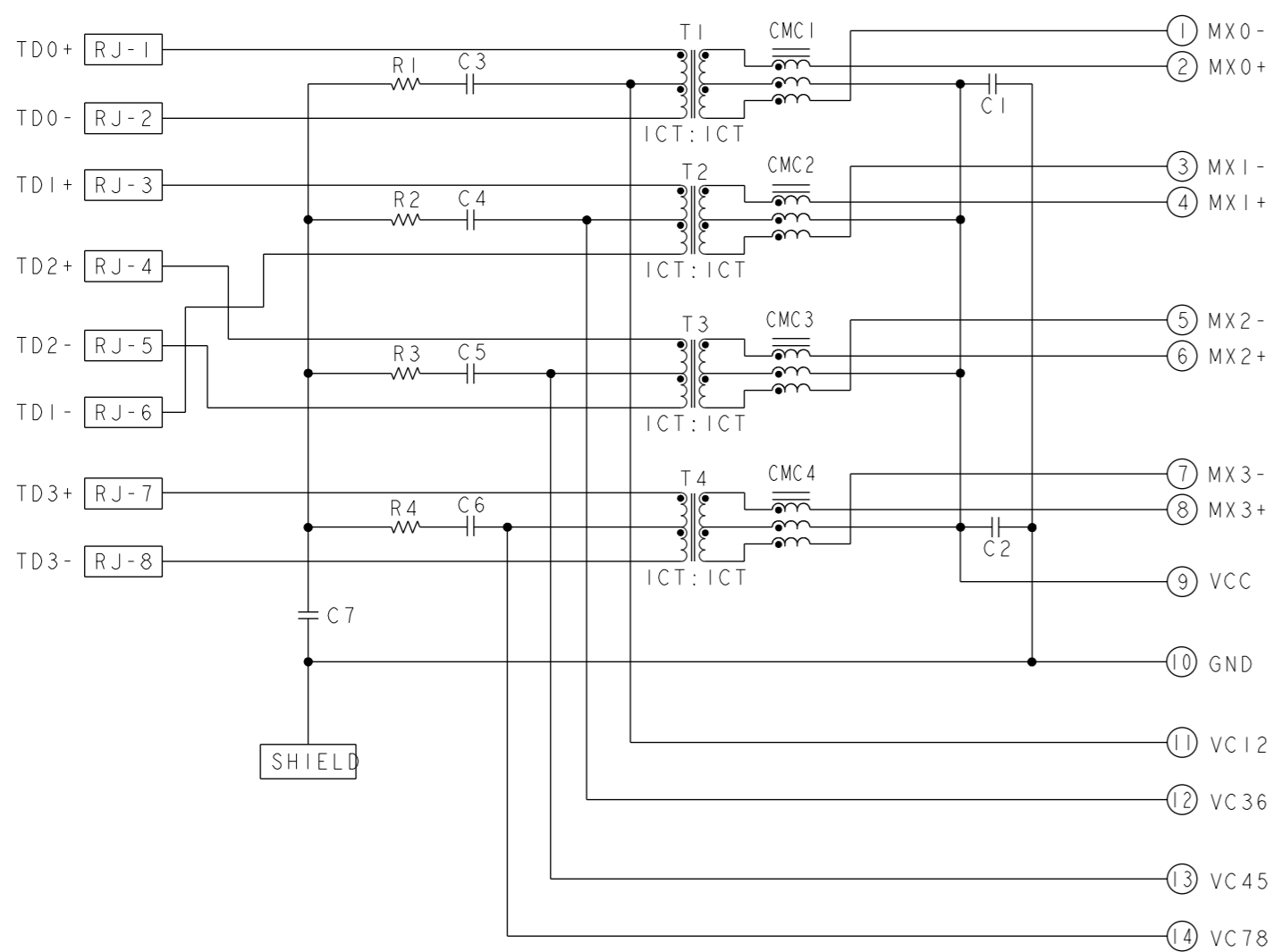


1. MATERIALS:
 PLASTIC HOUSING: BLACK, THERMOPLASTIC FLAMMABILITY RATING UL 94V-0
 SHIELD: BRASS, PREPLATED WITH 0.76um MIN SEMI-BRIGHT NICKEL,
 POST DIPPED WITH 2.54um MIN SAC SOLDER OR PURE TIN SOLDER
 ON SOLDER TAILS
 CONTACTS: PHOSPHOR BRONZE, 1.27um MIN OVERALL NICKEL
 UNDERPLATE WITH SELECT 1.27um MIN GOLD OR WITH SELECT 0.05um
 MIN GOLD OVER 0.76 um MIN PALLADIUM-NICKEL AT MATING INTERFACE
 AND 2.54um MIN MATTE TIN ON SOLDER TAILS.
2. MAGNETICS (PORT A, PORT C, PORT E AND PORT G)
 APPLICATION: 10/100/1000 BASE-T, ULTRA PoE PLUS
 IMPEDANCE: 100 OHMS
 TURNS RATIO (CHIP:CABLE): 1:1 ALL FOUR PAIRS
 OPEN CIRCUIT INDUCTANCE (OCL): ALL CHANNELS
 350uH MIN @ 100KHz, 0.1 VRMS WITH 8mA DC BIAS FROM 0°C TO 70°C
 120uH MIN @ 100KHz, 0.1 VRMS WITH 19mA DC BIAS FROM 0°C TO 70°C
 ALL FOUR PAIRS BI-DIRECTIONAL
 POE CURRENT: 600mA DC MAX
 PERFORMANCE @ 25°C:
 INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz
 RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 40MHz
 12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz
 CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz
 33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz
 COMMON MODE REJECTION RATIO (CMRR): 30dB MIN FROM 0.5MHz TO 100MHz
 ISOLATION VOLTAGE: 2250VDC(MAX) FOR 60 SECONDS WITH A RISE TIME OF
 500V/SEC AND WITH ALL PORTS CONNECTED.
3. PART NUMBER, DATE CODE AND COUNTRY OF ORIGIN ARE LOCATED
 IN APPROXIMATE AREA SHOWN. DATE CODE: "YY" IS YEAR, "WW" IS
 WORK WEEK, "D" IS DAY OF WEEK, WITH SUNDAY=1
4. TRP LOGO AND AGENCY APPROVAL LOGO ARE
 LOCATED IN APPROXIMATE AREA SHOWN.

5. OPERATING TEMP: FROM 0°C TO +70°C.
6. RJ45 CAVITY CONFORMS TO FCC RULES AND REGULATION PART 68 SUBPART F.
7. INDICATED MAGNETIC CONNECTIONS ARE SYMMETRICAL AND
 SUPPORT AUTO-MDI/MDIX.
8. DATUM AND BASIC DIMENSION ESTABLISHED BY CUSTOMER.
9. BASIC DIMENSION ESTABLISHED BY CUSTOMER, BUT MAY NOT BE
 GREATER THAN 5.08mm.
11. THE PARTS ARE RECOMMENDED FOR WAVE SOLDERING PROCESS,
 PEAK TEMPERATURE 260°C MAX, 10 SECONDS MAX.
12. MAGNETICS (PORT B, PORT D, PORT F AND PORT H)
 APPLICATION: 10/100/1000 BASE-T
 IMPEDANCE: 100 OHMS
 TURNS RATIO (CHIP:CABLE): 1:1 ALL FOUR PAIRS
 OPEN CIRCUIT INDUCTANCE (OCL):
 350uH MIN @100kHz, 0.1VRMS, 8mADC BIAS
 FROM 0°C TO 70°C, ALL FOUR PAIRS
 ALL FOUR PAIRS BI-DIRECTIONAL
 PERFORMANCE @ 25°C:
 INSERTION LOSS (IL): 1.1dB MAX FROM 0.5MHz TO 100MHz
 RETURN LOSS (RL): 18dB MIN FROM 0.5MHz TO 40MHz
 12-20LOG(f/80)dB MIN FROM 40.1MHz TO 100MHz
 CROSSTALK ATTENUATION: 35dB MIN FROM 0.5MHz TO 40MHz
 33-20LOG(f/50)dB MIN FROM 40.1MHz TO 100MHz
 COMMON MODE REJECTION RATIO (CMRR):
 30dB MIN FROM 0.5MHz TO 100MHz
 ISOLATION VOLTAGE: 2250VDC (MAX) FOR 60 SECONDS WITH
 A RISE TIME OF 500V/SEC AND WITH ALL PORTS CONNECTED

S9HG154 GIGABIT UPoE CIRCUIT

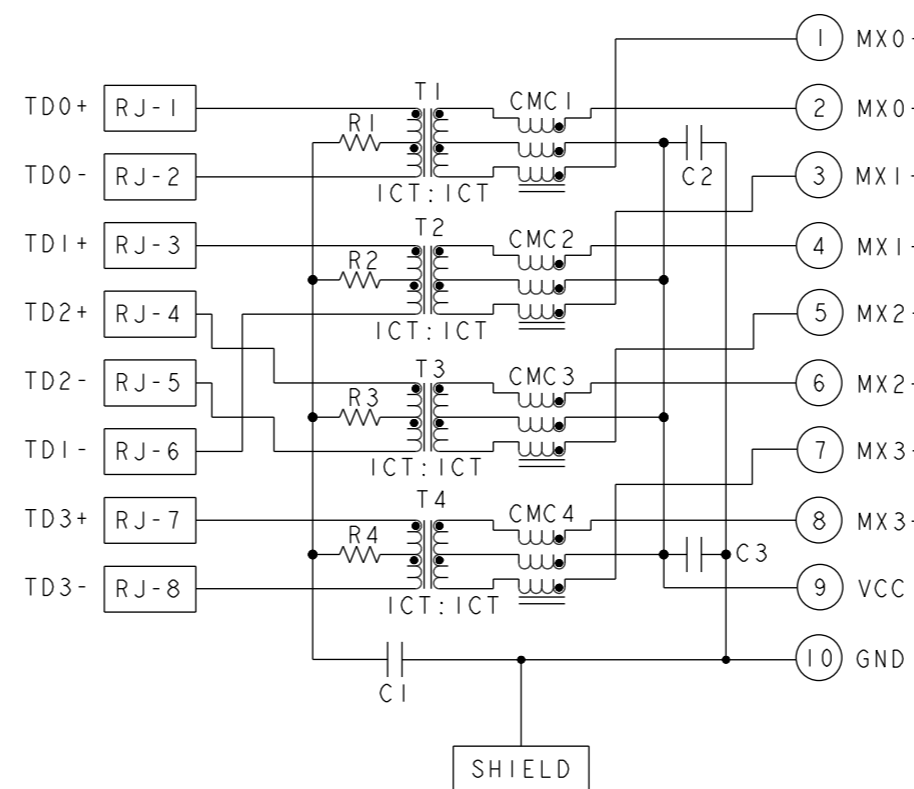
PORT A, PORT C, PORT E AND PORT G



C1-C2 = 10nF, 50V, X7R, CAPACITORS
 C3-C6 = 22nF, 100V, CAPACITORS
 C7 = 1000pF, 2kV, CAPACITOR
 R1-R4 = 75 Ohms, 1/16W, RESISTORS

S8G56 GIGABIT CIRCUIT

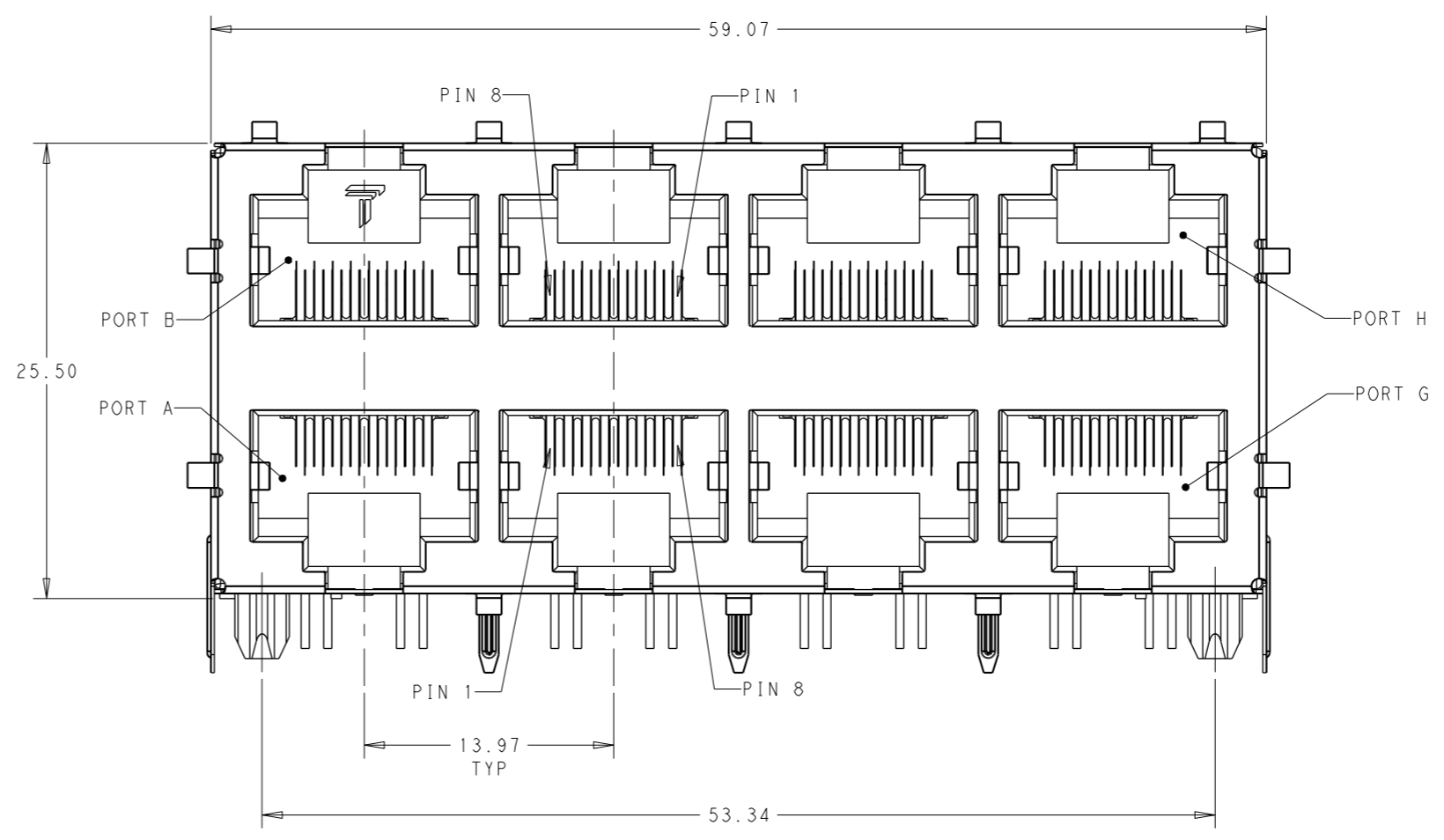
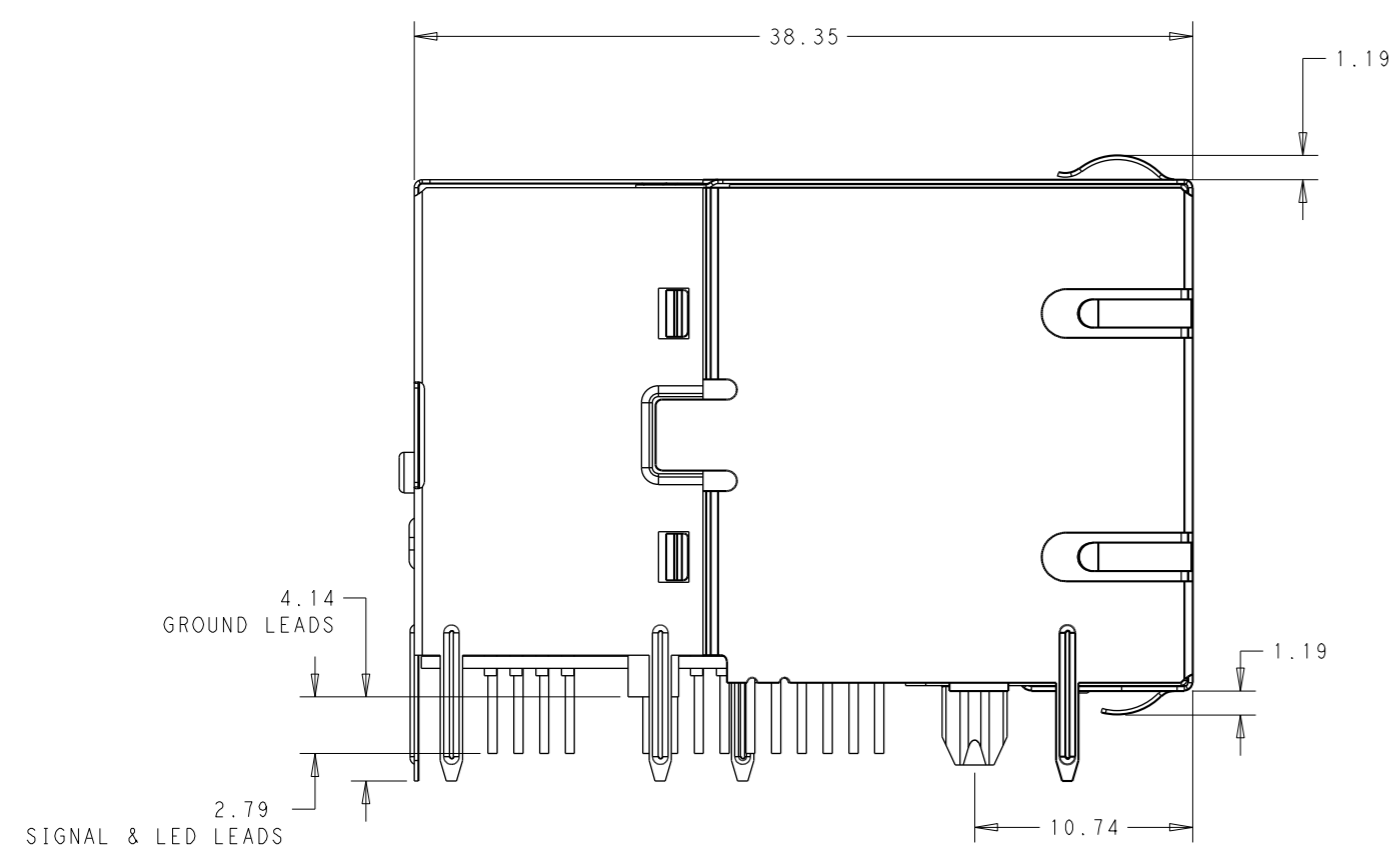
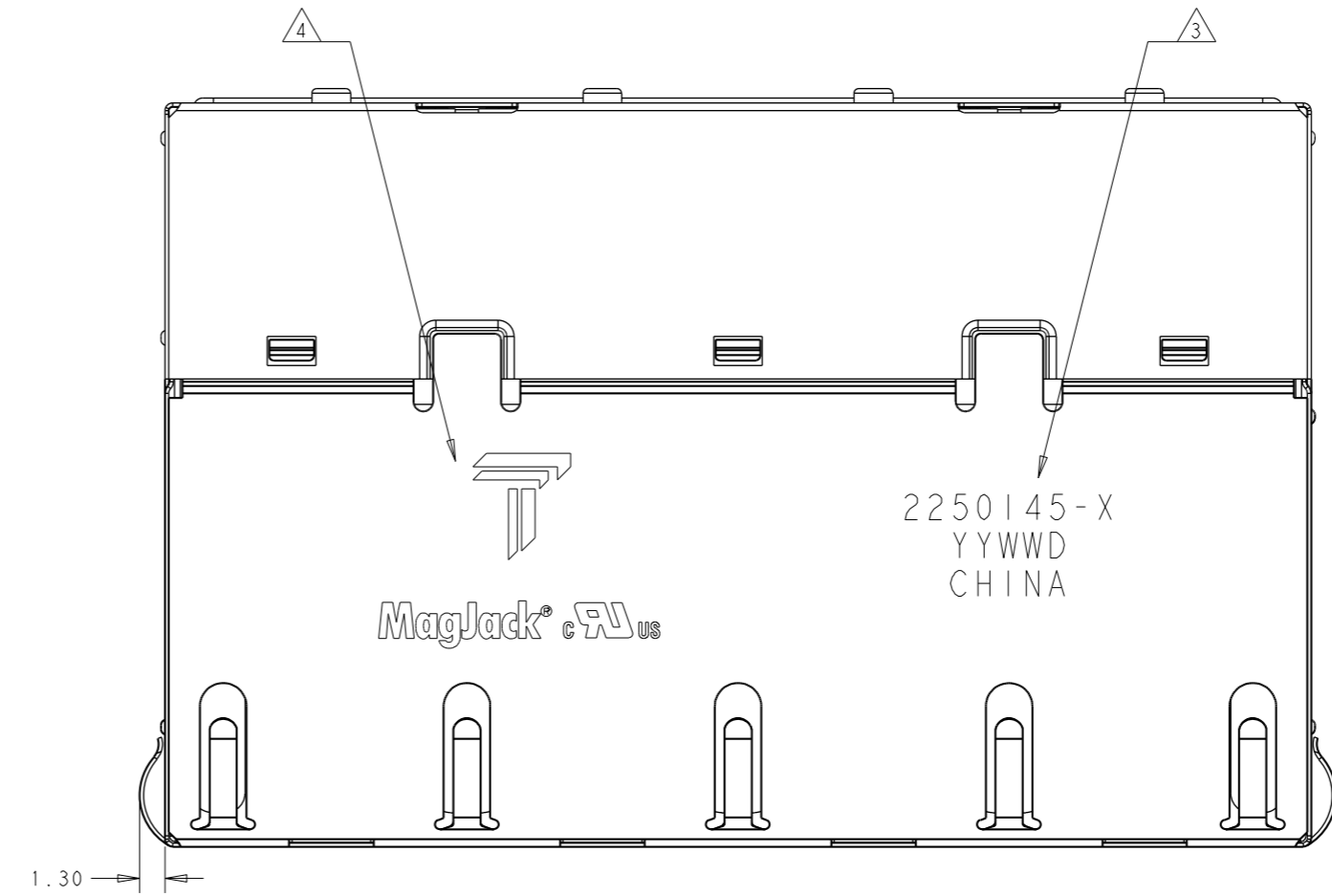
PORT B, PORT D, PORT F AND PORT H




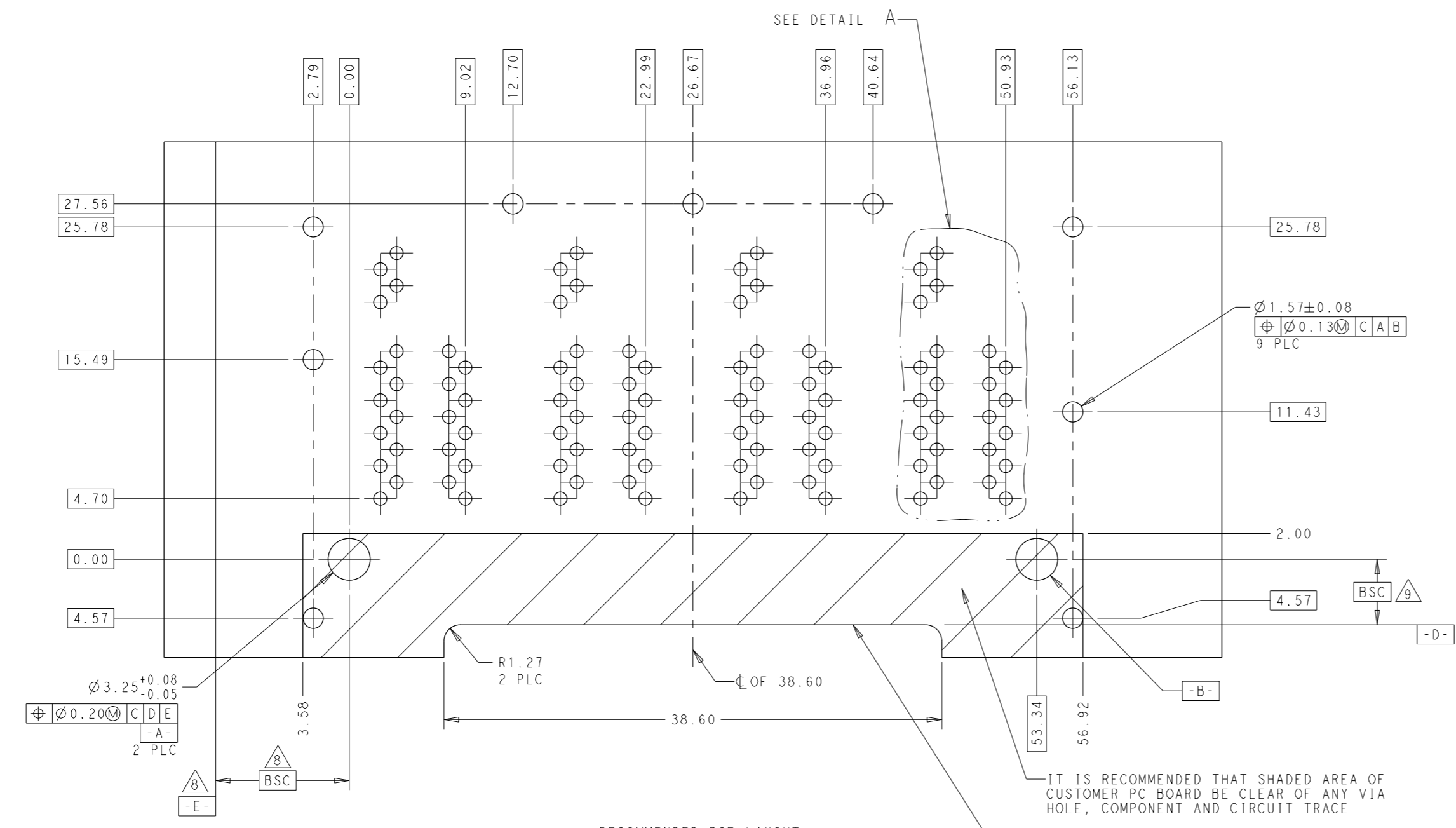
C1 = 1000pF, 2kV CAPACITOR
 C2-C3 = 10nF, 50V CAPACITORS
 R1-R4 = 75 Ohms, 1/16 W, RESISTORS

2250145-1
 PART
 NUMBER

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN: TOMMY REN/LEERY LIN 24JAN2014		trp CONNECTOR a bel group DONGGUAN CHINA
DIMENSIONS: mm		CHK: TOMMY REN 24JAN2014		
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APPD: TONY YUAN 24JAN2014		DESC: 2X4 S9HG154 GIGABIT UPoE CIRCUIT AND S8G56 GIGABIT CIRCUIT SIZE: A1 SCALE: NTS SHEET: 1 of 4 REV: 2
0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ±		MODEL NAME: MAGJACK STACK 4PPoE CUSTOMER DRAWING		
PRODUCT SPEC		APPLICATION SPEC		RESTRICTED TO

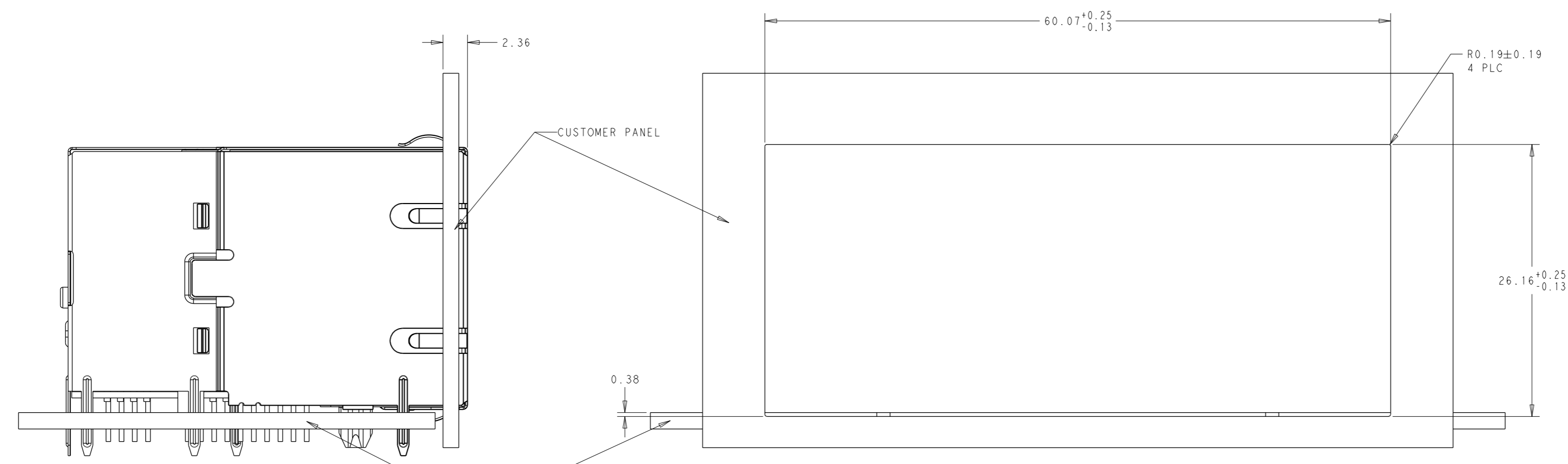
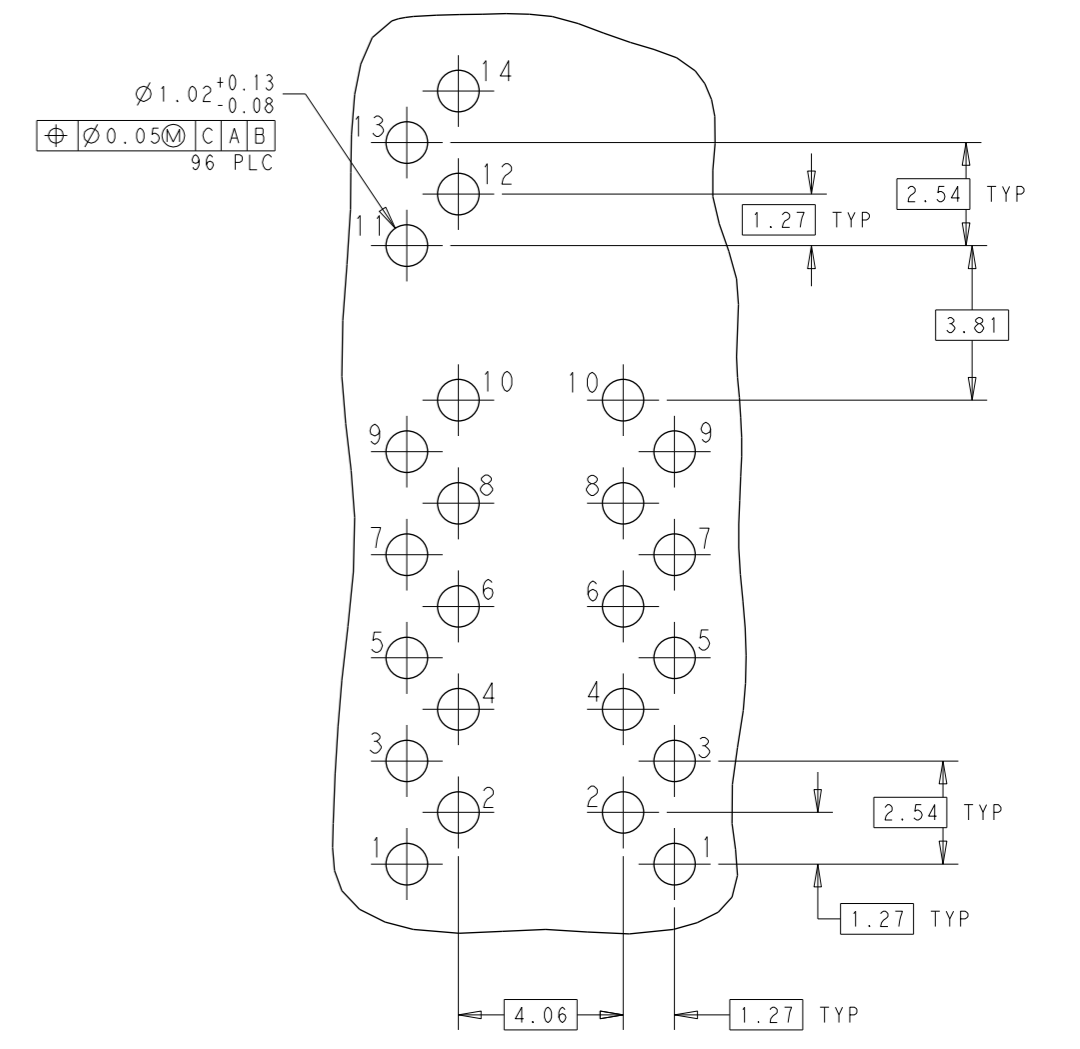


THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN: TOMMY REN/24 JAN 2014		 TRP CONNECTOR a bel group DONGGUAN CHINA
DIMENSIONS: mm		CHK: TOMMY REN/24 JAN 2014		
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APPV: TONY YUAN/24 JAN 2014		DESC: 2X4 S9HG154 GIGABIT UPoE CIRCUIT AND S8G56 GIGABIT CIRCUIT
0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ± APPLICATION SPEC ±		MODEL NAME: MAGJACK STACK 4PPoE		RESTRICTED TO: -
PRODUCT SPEC: -		SCALE: A1		SIZE: A1
CUSTOMER DRAWING		SCALE: NTS		SHEET 2 OF 4 REV 2

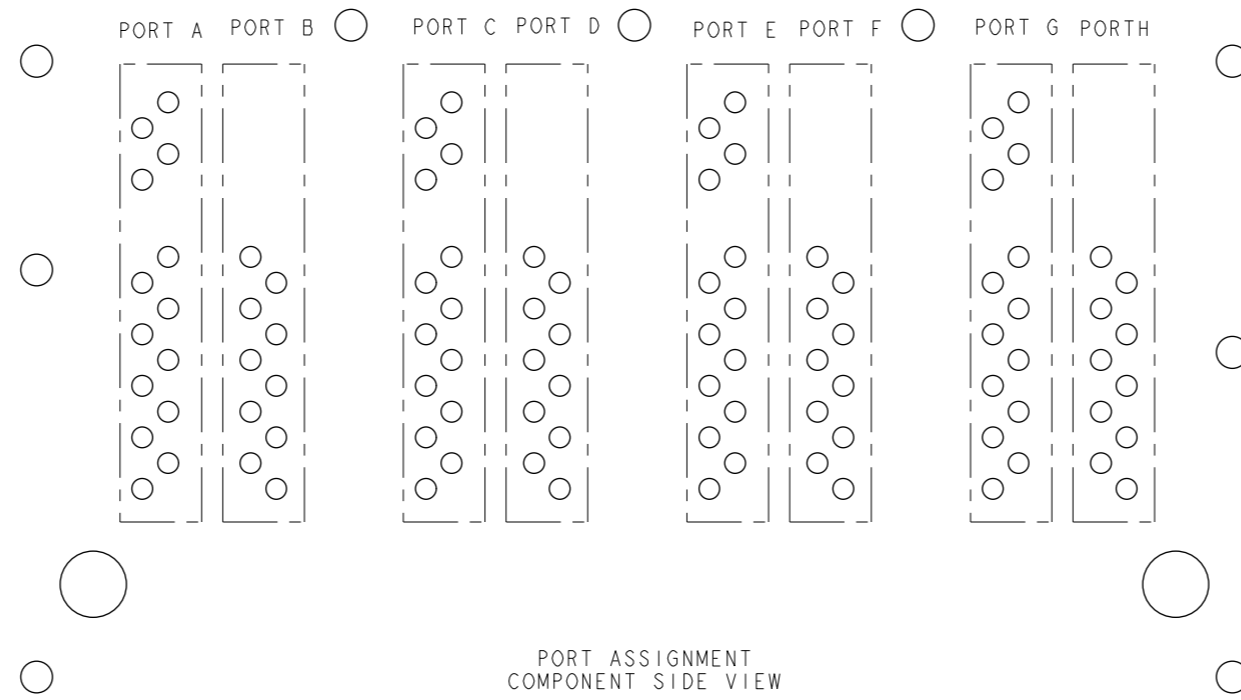


IT IS RECOMMENDED THAT SHADED AREA OF CUSTOMER PC BOARD BE CLEAR OF ANY VIA HOLE, COMPONENT AND CIRCUIT TRACE


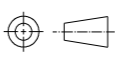
RECOMMENDED PCB FRONT EDGE CUTOUT: THE BOTTOM SHIELD GROUND TABS(FRONT) SHOULD NOT BE SEATED ON THE TOP OF THE PCB



THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN: TOMMY REN/TERRY LIN 24JAN2014		 trp CONNECTOR DONGGUAN CHINA a bel group
DIMENSIONS: mm		CHK: TOMMY REN 24JAN2014		
TOLERANCES UNLESS OTHERWISE SPECIFIED:		APPV: TONY YUAN 24JAN2014		MODEL NAME: MAGJACK DESC: 2X4 S9HG154 GIGABIT UPoE CIRCUIT AND S8G56 GIGABIT CIRCUIT SIZE: A1 CAGE CODE: C=2250145 DRAWING NO: 2250145
0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ± APPLICATION SPEC ±		MODEL NAME: MAGJACK DESC: 2X4 S9HG154 GIGABIT UPoE CIRCUIT AND S8G56 GIGABIT CIRCUIT SIZE: A1 CAGE CODE: C=2250145 DRAWING NO: 2250145		
PRODUCT SPEC		CUSTOMER DRAWING		RESTRICTED TO: - SCALE: NTS SHEET: 3 OF 4 REV: 2



PORT ASSIGNMENT COMPONENT SIDE VIEW

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN: TOMMY REN/IEBRY LIN 24 JAN 2014		 trp CONNECTOR a bel group DONGGUAN CHINA
		CHK: TOMMY REN 24 JAN 2014		
DIMENSIONS: mm		TOLERANCES UNLESS OTHERWISE SPECIFIED:		APPR: TONY YUAN 24 JAN 2014
		0 PLC ±0.25 1 PLC ±0.25 2 PLC ±0.25 3 PLC ± 4 PLC ± ANGLES ± APPLICATION SPEC ±		MODEL NAME: MAGJACK STACK 4Ppoe
PRODUCT SPEC		APPLICATION SPEC		DESC: 2X4 S9HG154 GIGABIT UPoE CIRCUIT AND S8G56 GIGABIT CIRCUIT
-		-		SIZE: A1
CUSTOMER DRAWING		SCALE: NTS		RESTRICTED TO: -
		SHEET 4 OF 4		REV 2